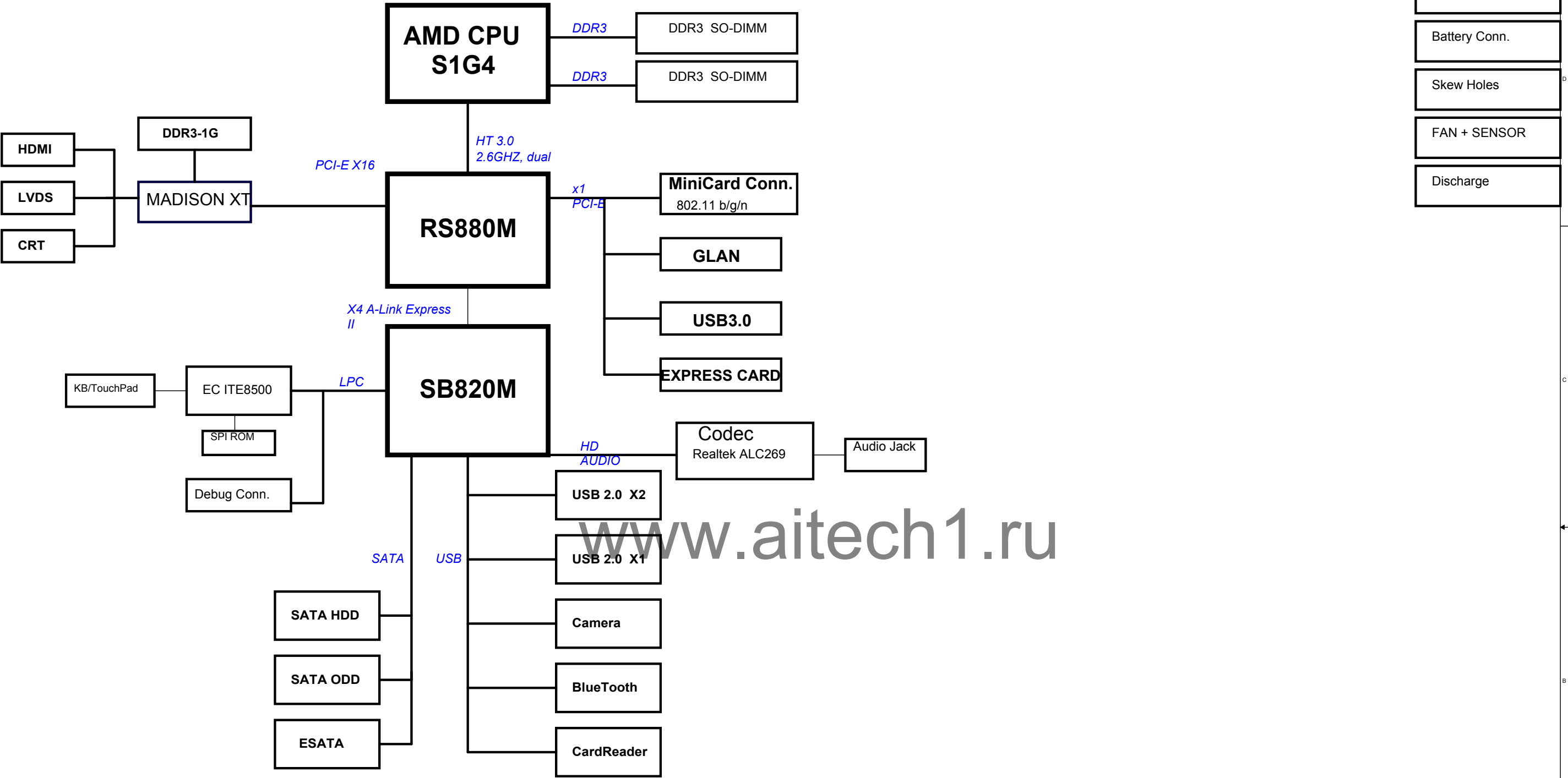


N61Da  
Block Diagram



## SB820M GPIO

[illegible]

**EC IT8500**

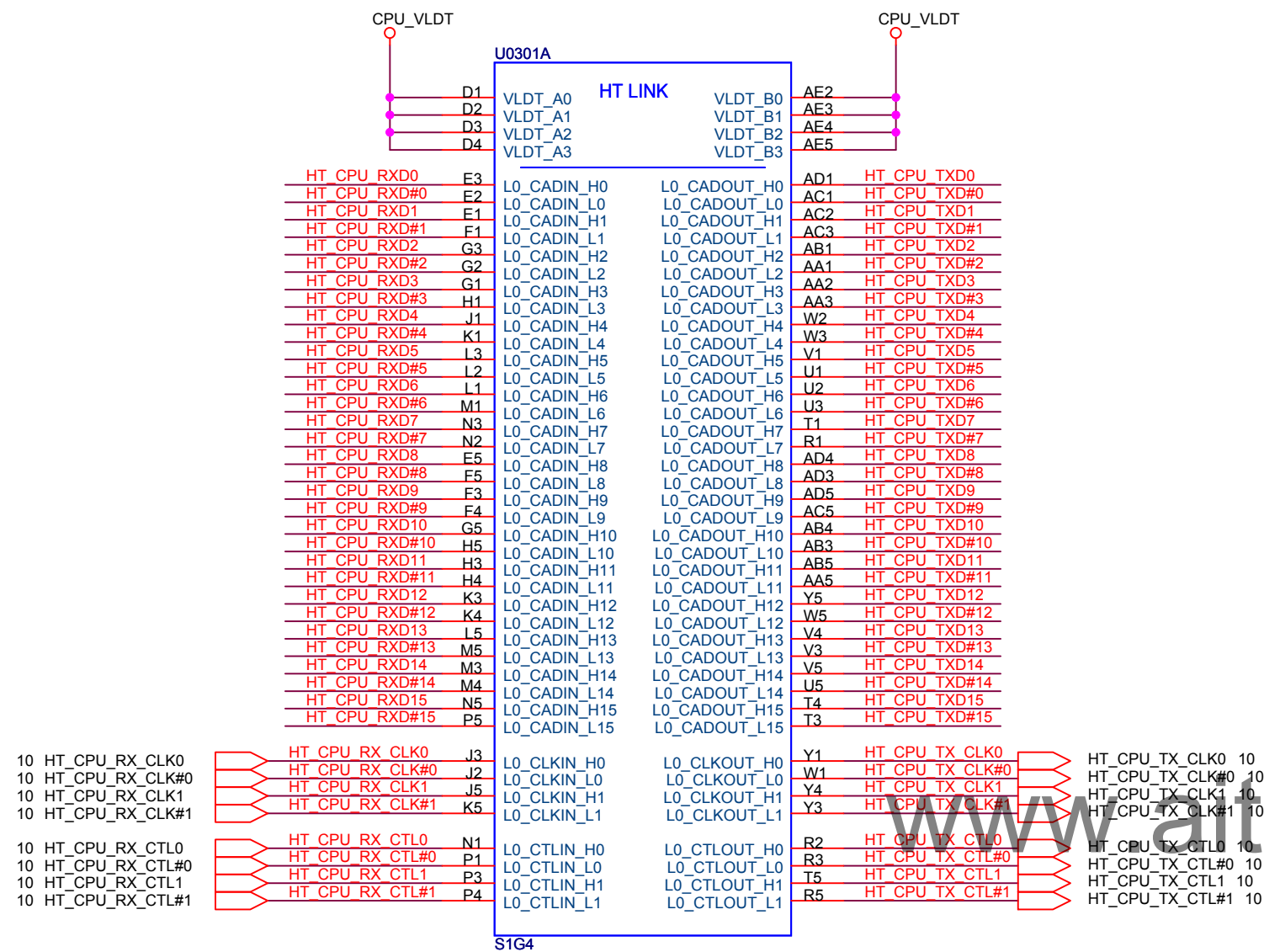
EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	CHG_FULL_LED#	
GPA3	-	-	
GPA4	GPO	EC_LCD_BL_PWM	
GPA5	GPO	FAN_PWM	
GPA6	-	-	
GPA7	-	-	
GPB0	GPO	BATSEL_0	
GPB1	GPO	BATSEL_1	
GPB2	-	-	
GPB3	ALT	SMB0_CLK_EC	
GPB4	ALT	SMB0_DAT_EC	
GPB5	GPO/OD	A20GATE_EC	
GPB6	GPO/OD	RC_IN#_EC	
GPB7	GPO	PM_RSMRST#_EC	
GPC0	-	-	
GPC1	ALT	SMB1_CLK_EC	
GPC2	ALT	SMB1_DAT_EC	
GPC3	GPO	PM_PWRBTN#	
GPC4	GPI	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	-	-	
GPD0	GPI	PWRLIMIT#	
GPD1	GPI	PM_SUSC#	
GPD2	GPI	BUF_PLT_RST#_EC	
GPD3	GPO/OD	EC_SCI#	
GPD4	GPO/OD	EC_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	GPI	FAN_TACH	
GPD7	-	-	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	GPI	PWR_SW#	
GPE5	-	-	
GPE6	GPI	LID_SW#	
GPE7	-	-	
GPF0	-	-	
GPF1	-	-	
GPF2	GPI	MARATHON#	
GPF3	-	-	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	EC_LPCRST_GATE#	
GPG0	-	-	
GPG1	GPI	PM_SUSB#	
GPG2	-	-	
-	-	-	
-	-	-	

**SM\_BUS ADDRESS :**

SM-Bus Device	SM-Bus Address
SO-DIMM 0	TBD
SO-DIMM 1	TBD

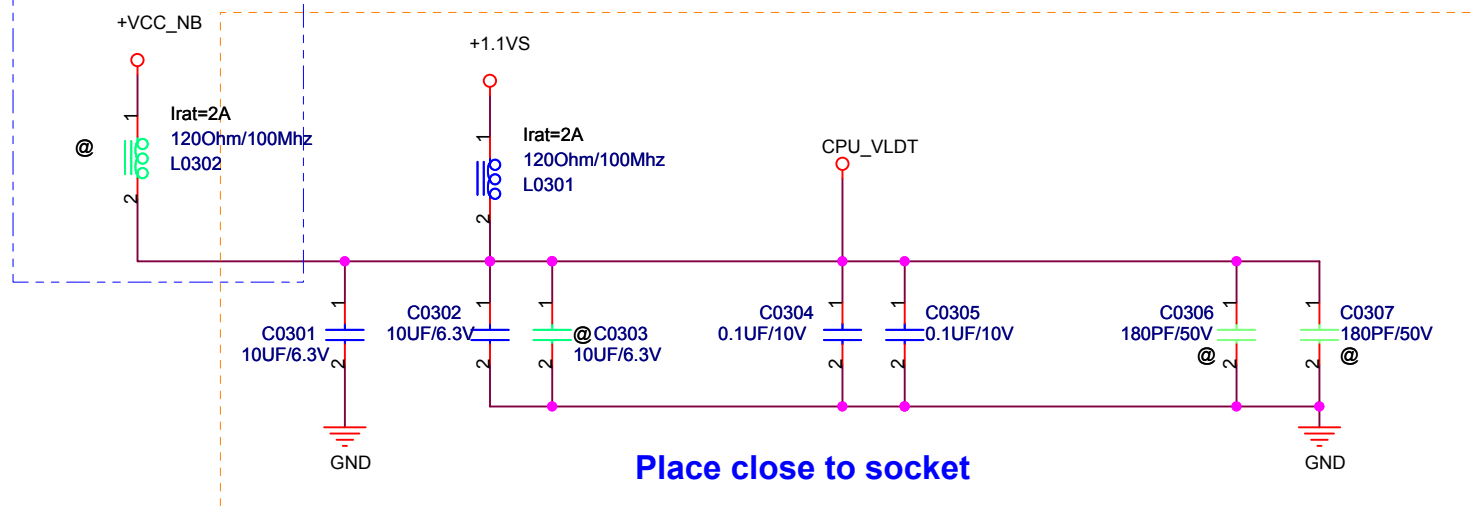
[illegible]

HyperTransport I/O power supply  
(VLDT: 1.5A@1.1V)



P/N: 12G011306380

R1.2 for power seq.



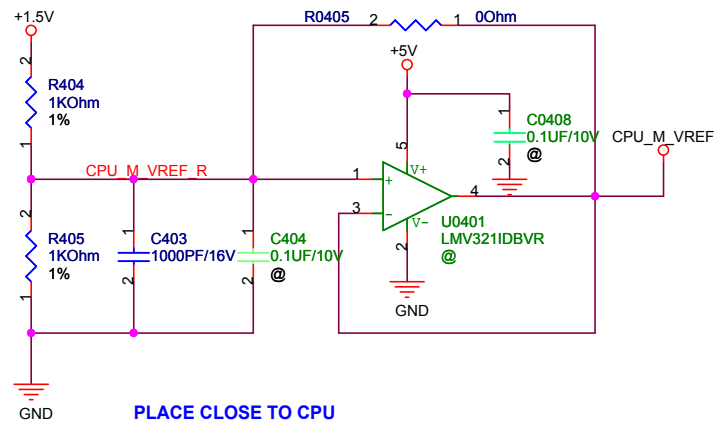
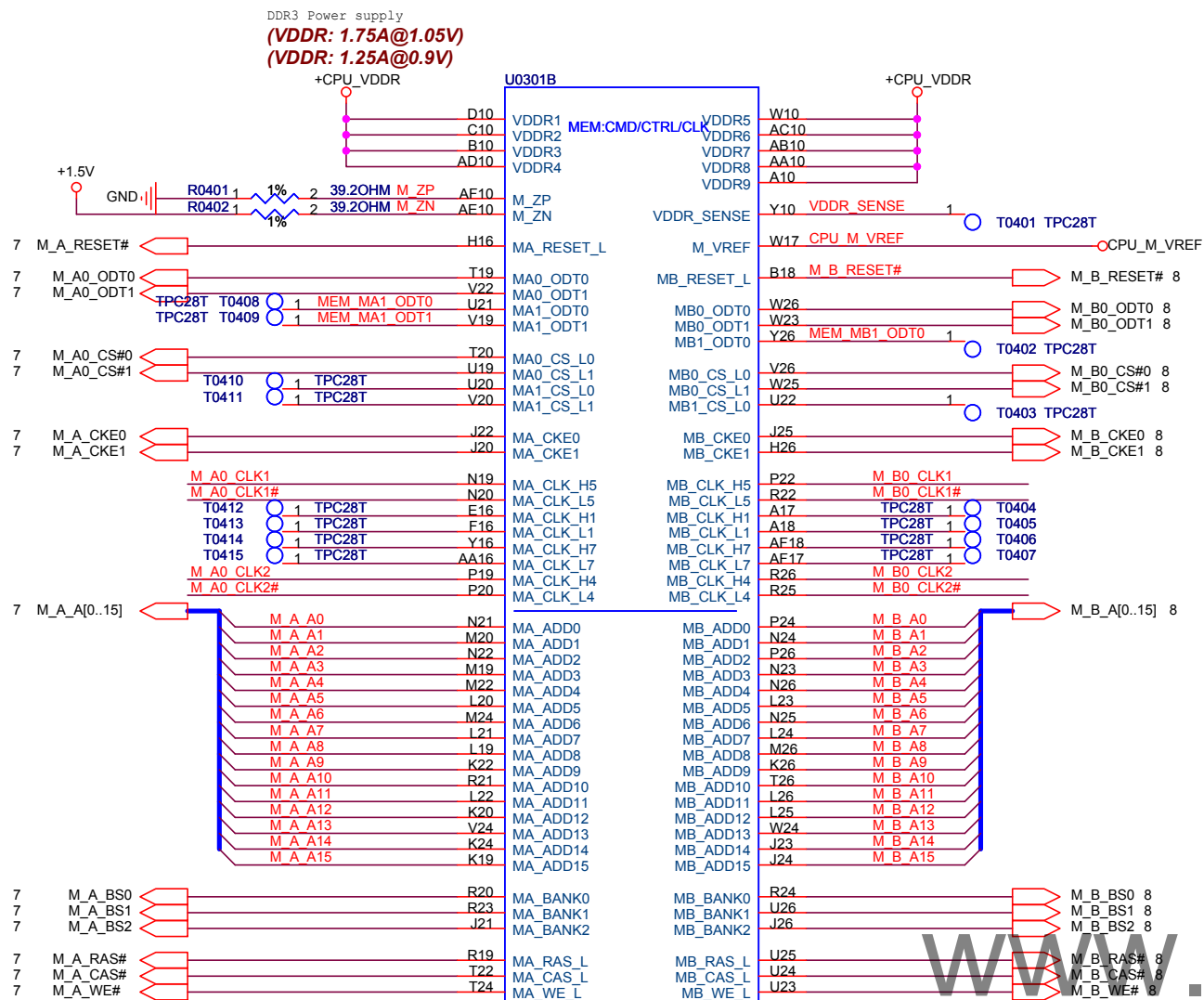
HT\_CPU\_TXD[0..15] 10

HT\_CPU\_TXD#[0..15] 10

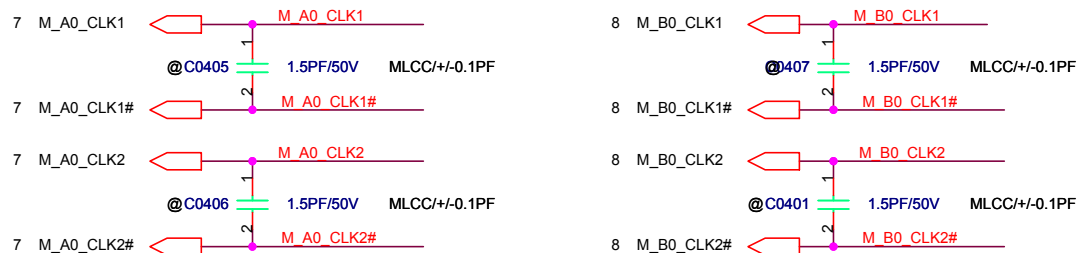
10 HT\_CPU\_RXD[0..15]

10 HT\_CPU\_RXD#[0..15]

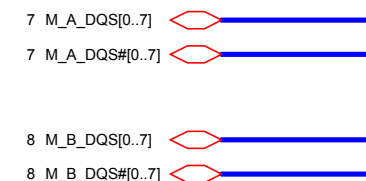
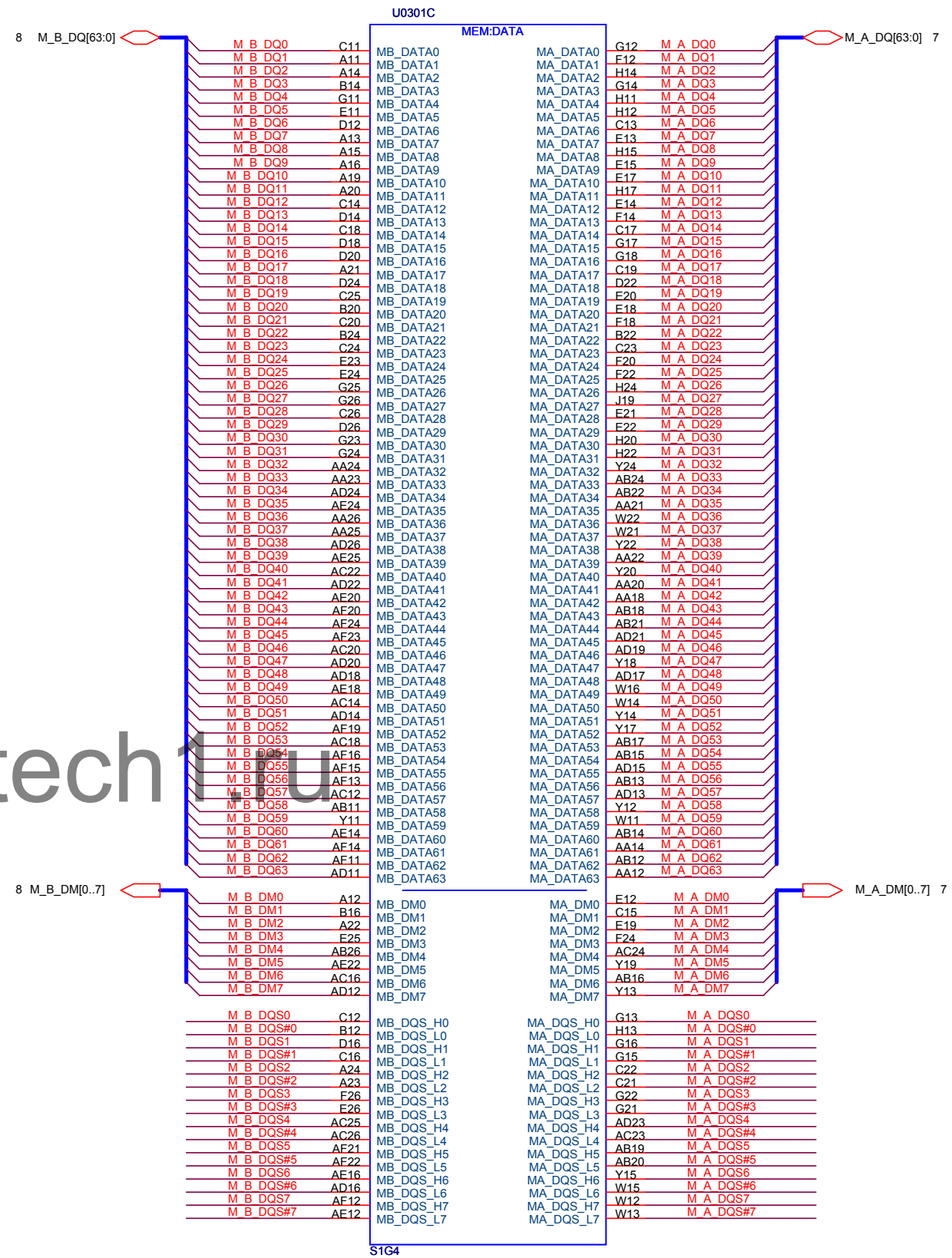
ASUS		Title : S1g4-HT I/F	
ASUSTeK.Computer.INC		Engineer: Uei Lee	
Size B	Project Name N61Da		Rev 1.1
Date: Wednesday, March 31, 2010		Sheet 3 of 79	1



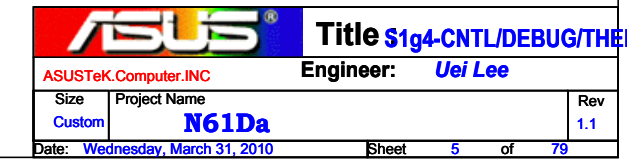
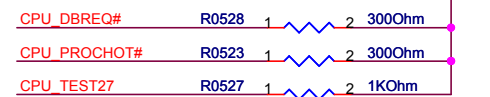
place close to RROCESSOR within 1.5 inch



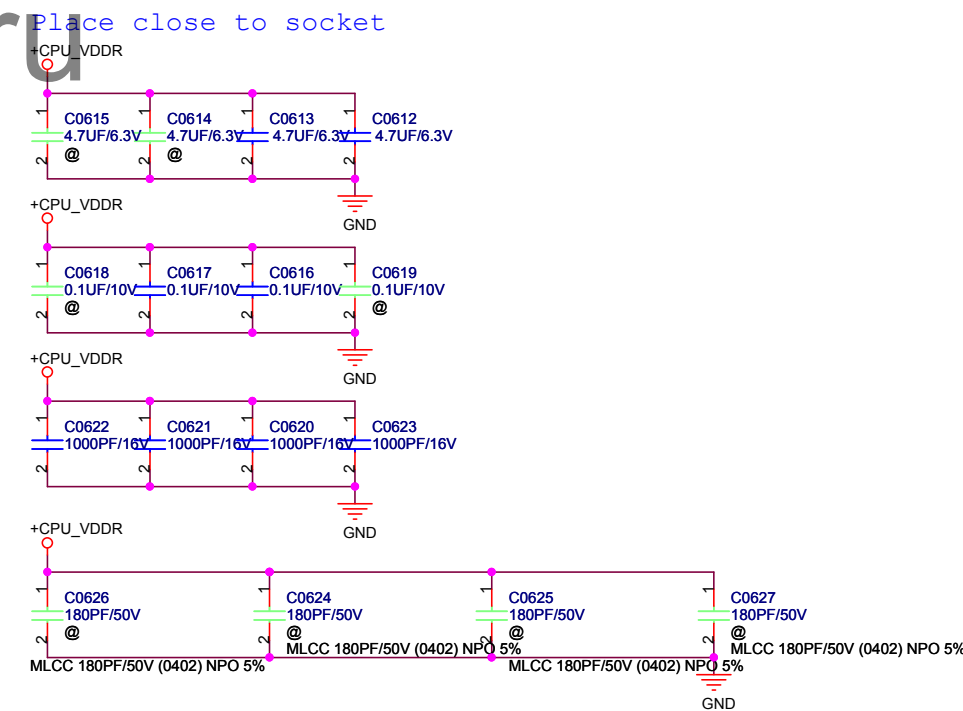
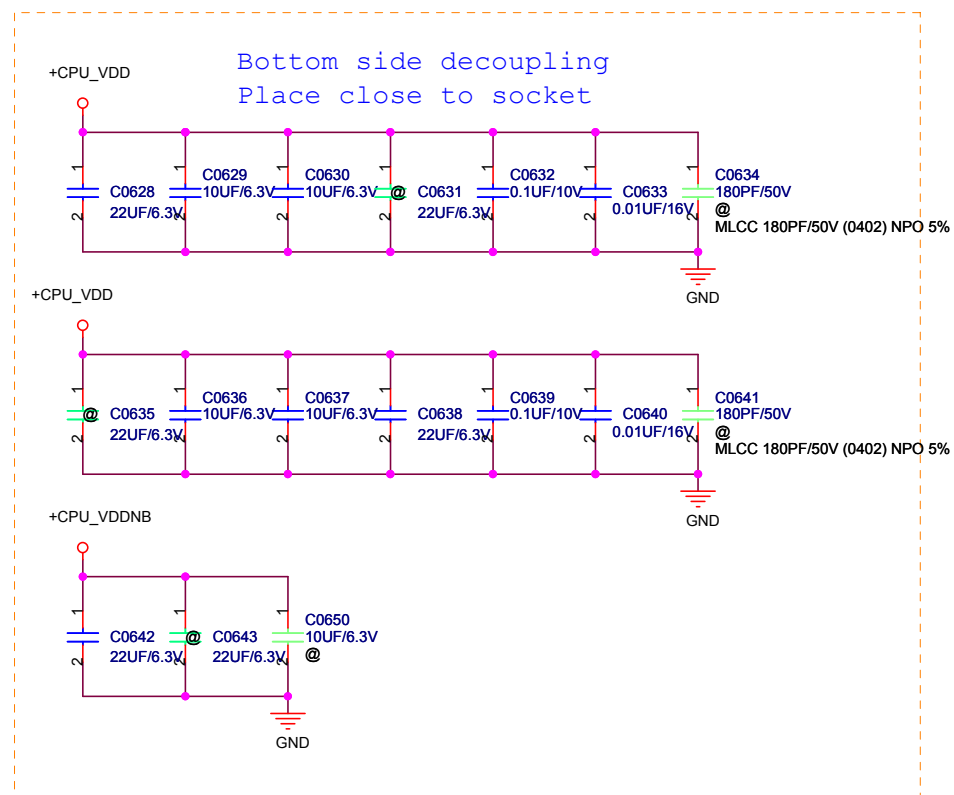
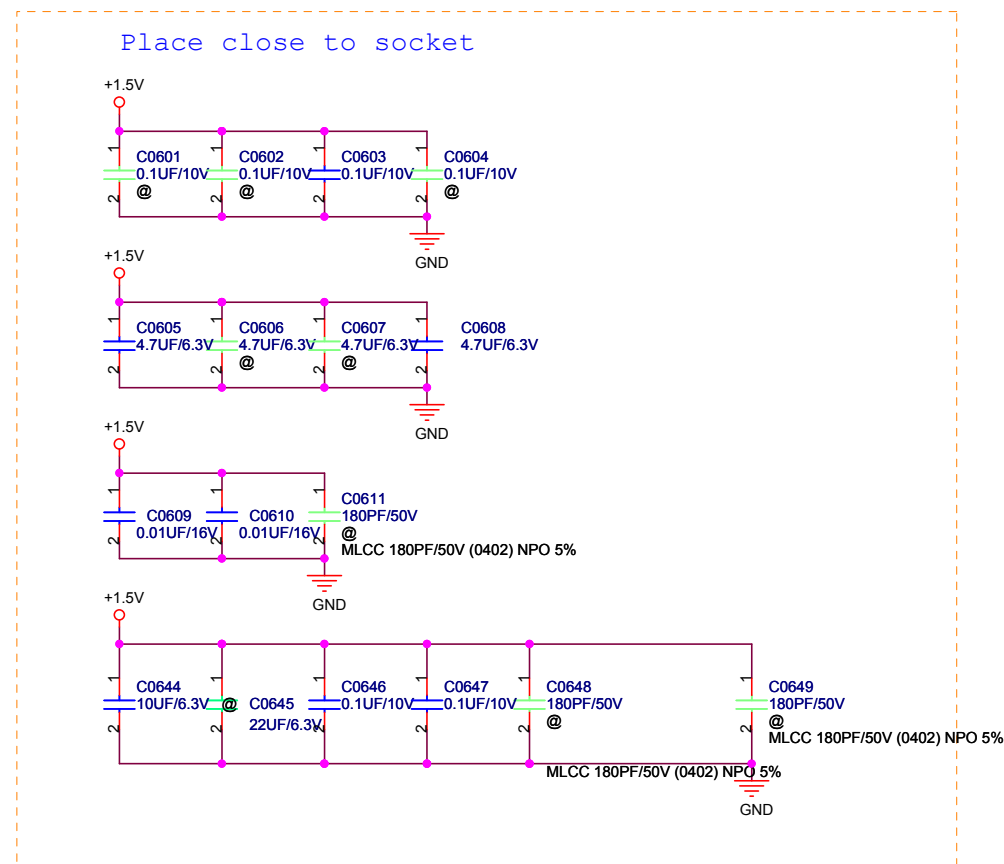
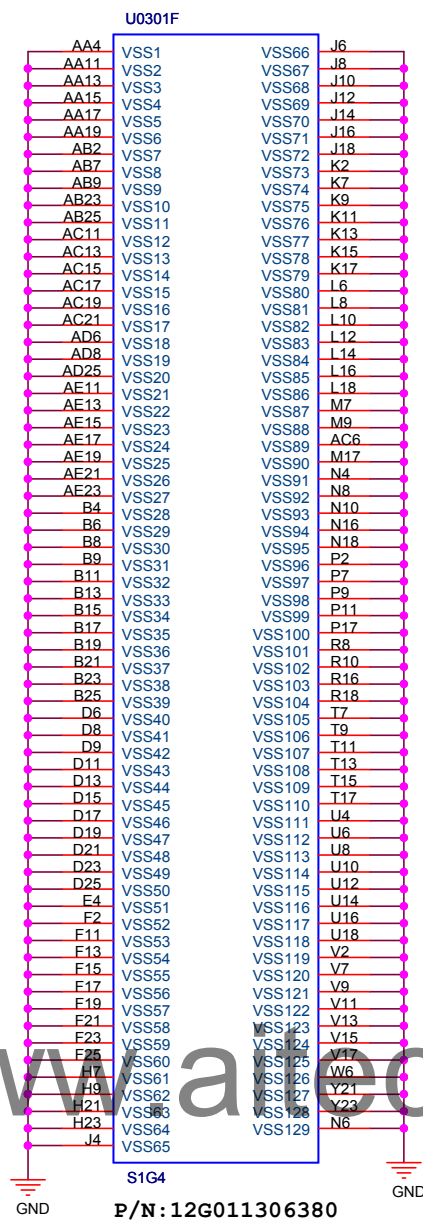
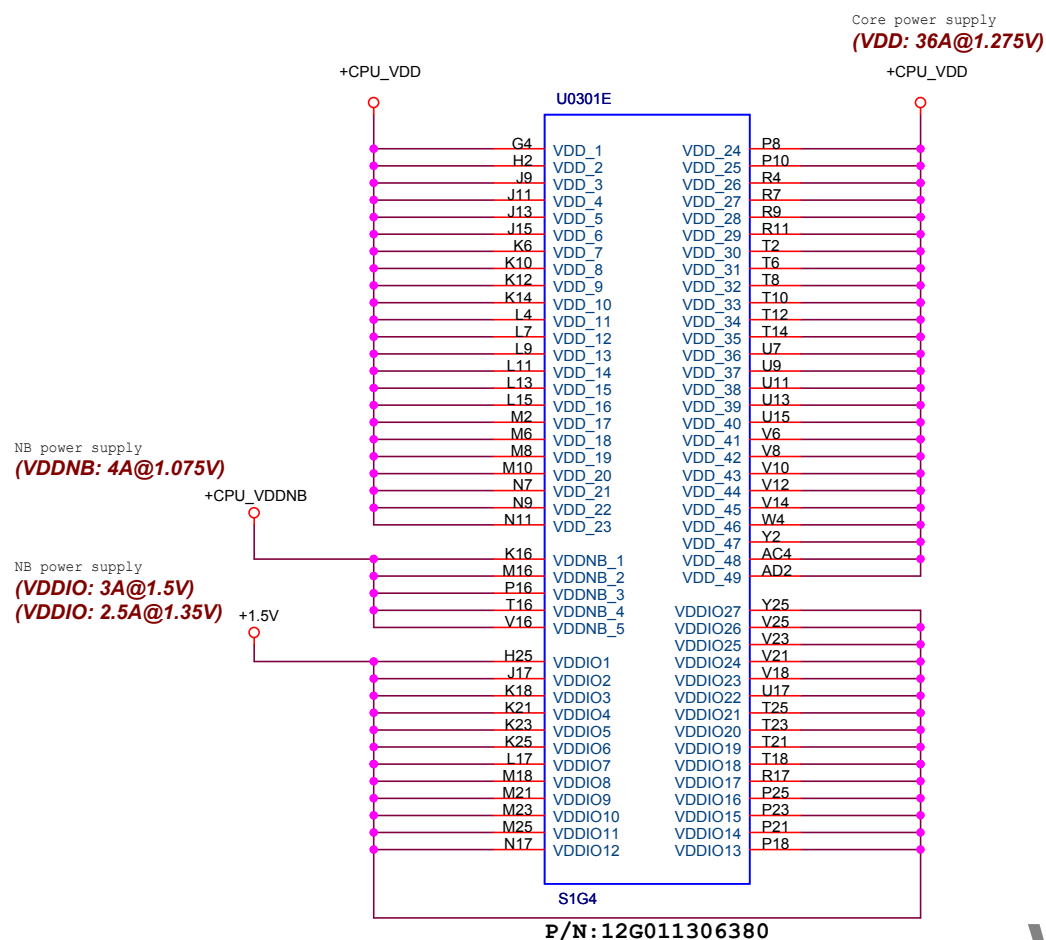
## Processor Memory Interface

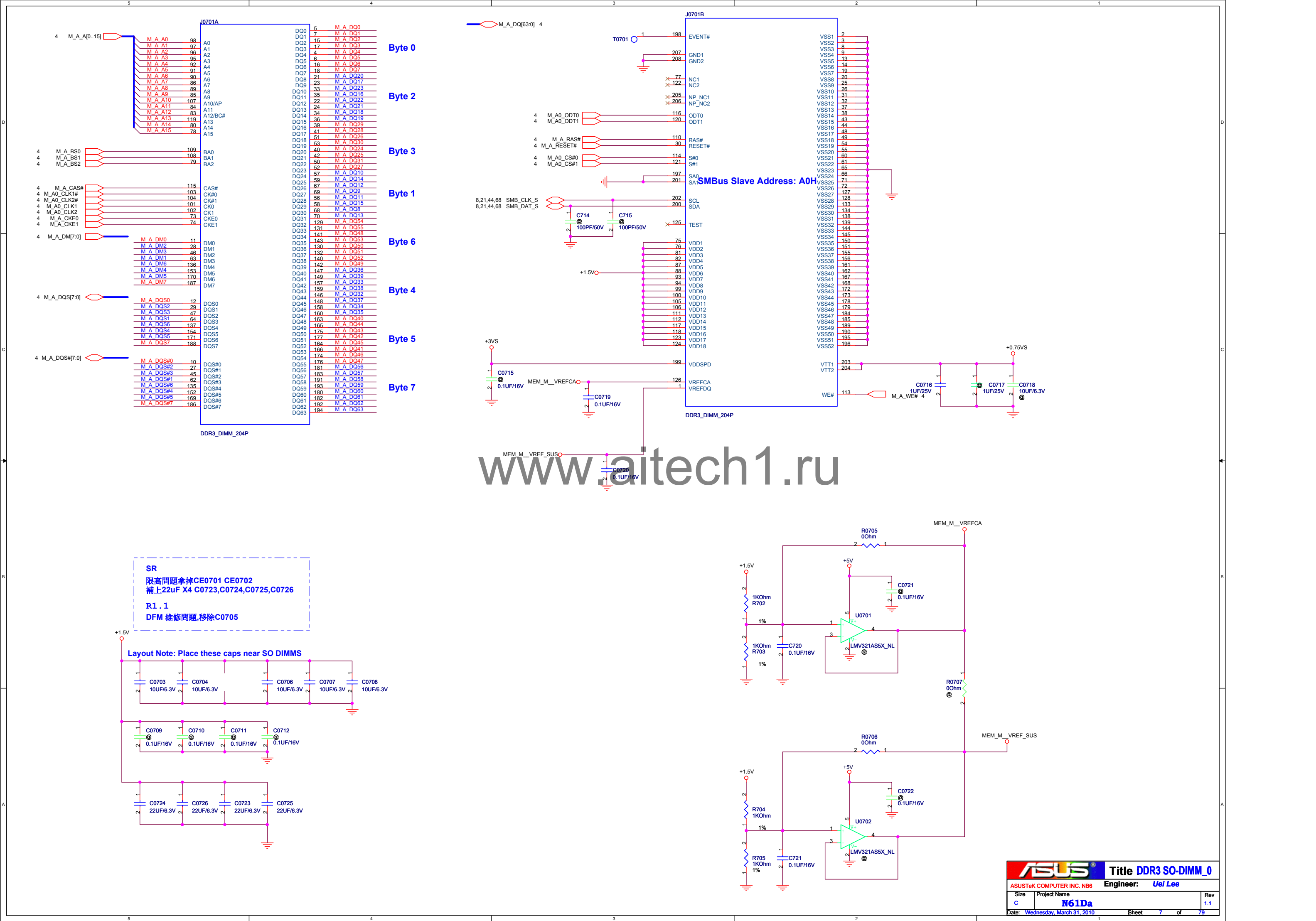


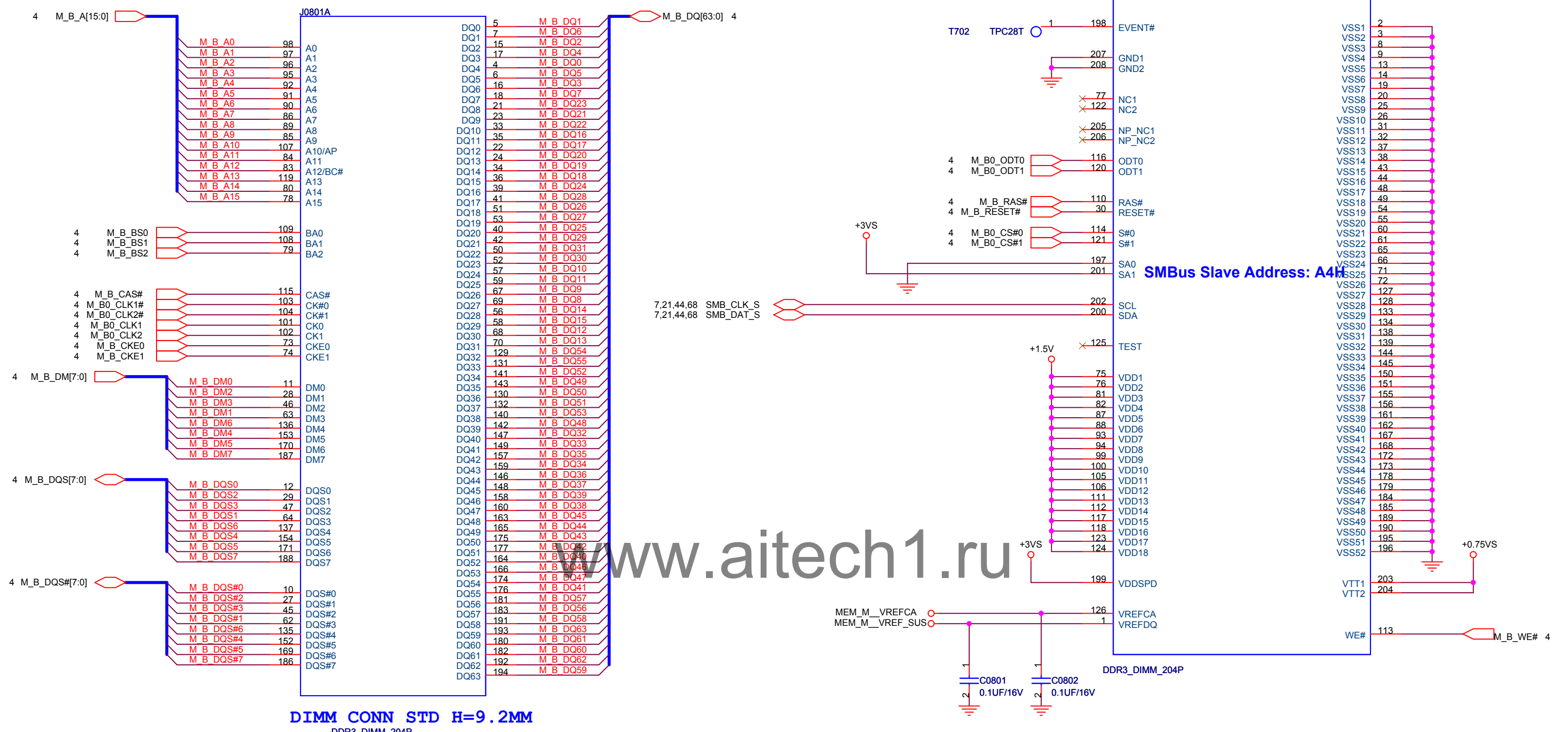
## VID setting












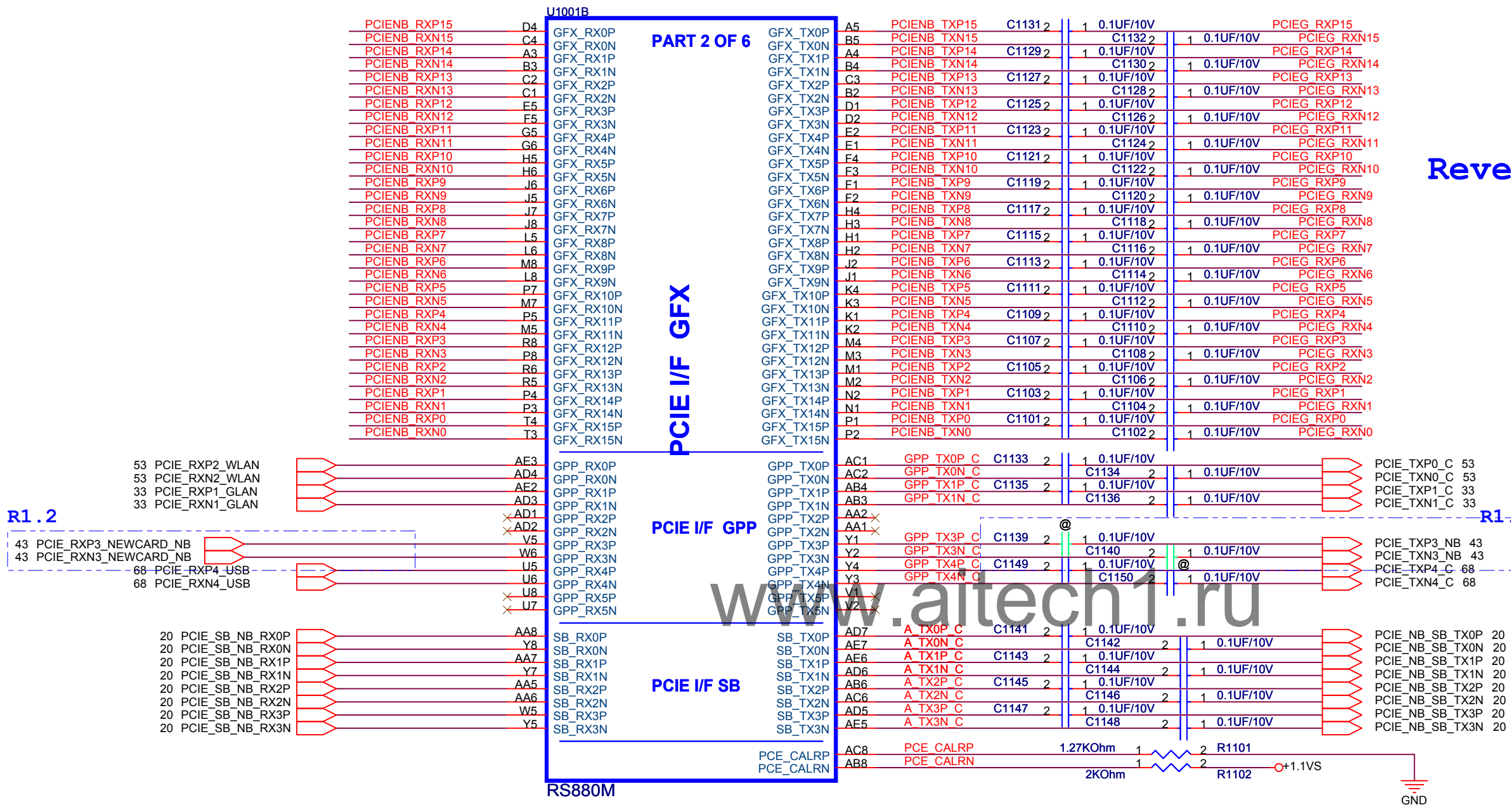


**Main Board**

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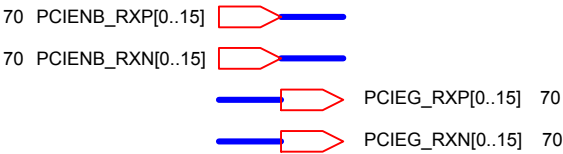
		<b>Title :</b> NB_****	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> Uei Lee	
Size A	Project Name N61Da		Rev 1.0
Date: Tuesday, March 30, 2010		Sheet 9 of 79	



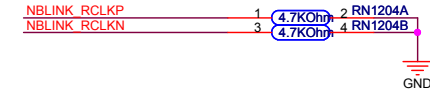
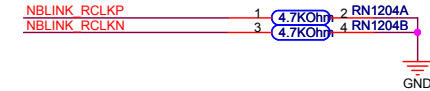
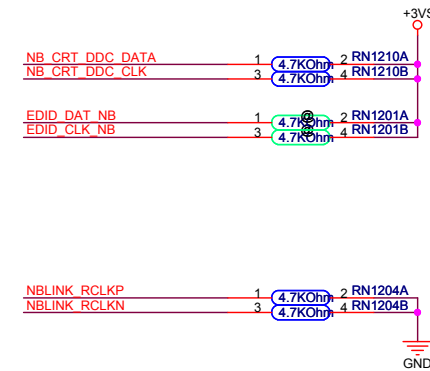
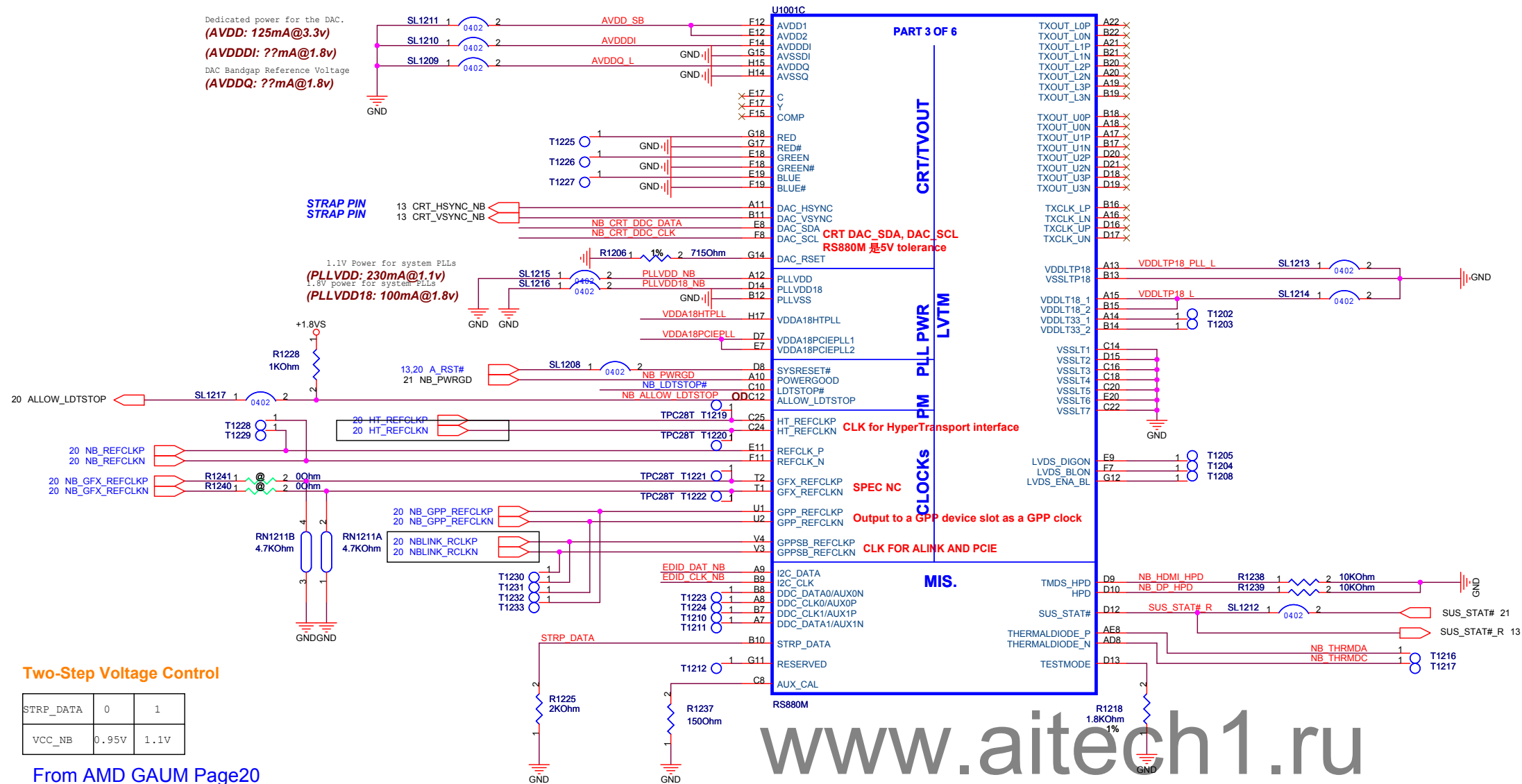


Reverse PCIE 16 lane

PCIE PORT	DEVICE
PORT0	WLAN
PORT1	LAN
PORT2	NC
PORT3	Express Card
PORT4	USB3.0



Dedicated power for the DAC.  
(AVDD: 125mA@3.3v)  
(AVDDI: ??mA@1.8v)  
DAC Bandgap Reference Voltage  
(AVDDQ: ??mA@1.8v)



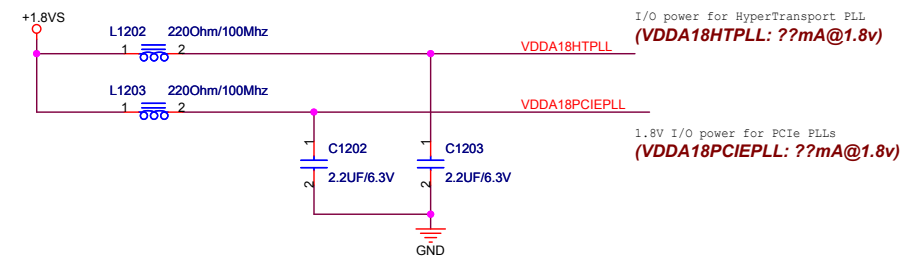
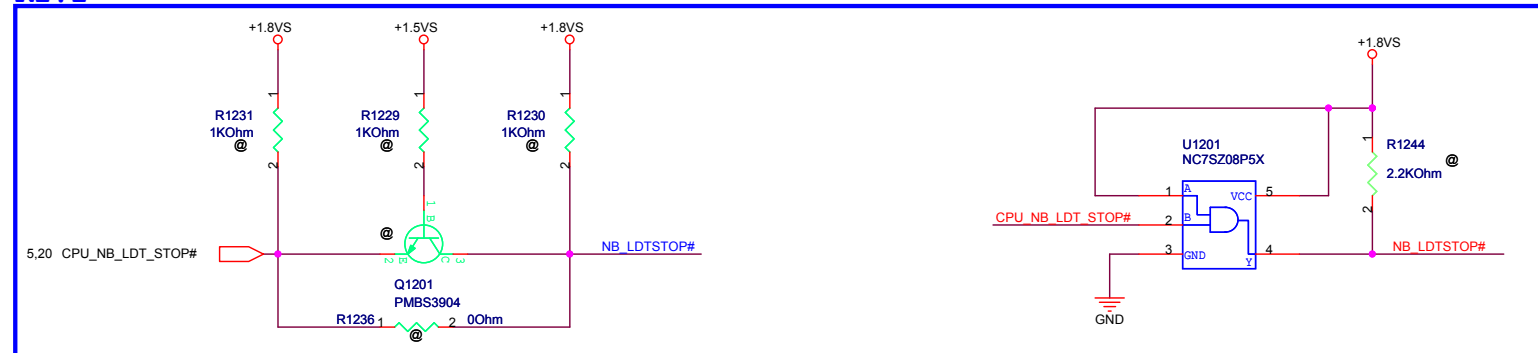
#### Two-Step Voltage Control

STRP_DATA	0	1
VCC_NB	0.95V	1.1V

From AMD GAUM Page20  
NB CLOCK INPUT TABLE

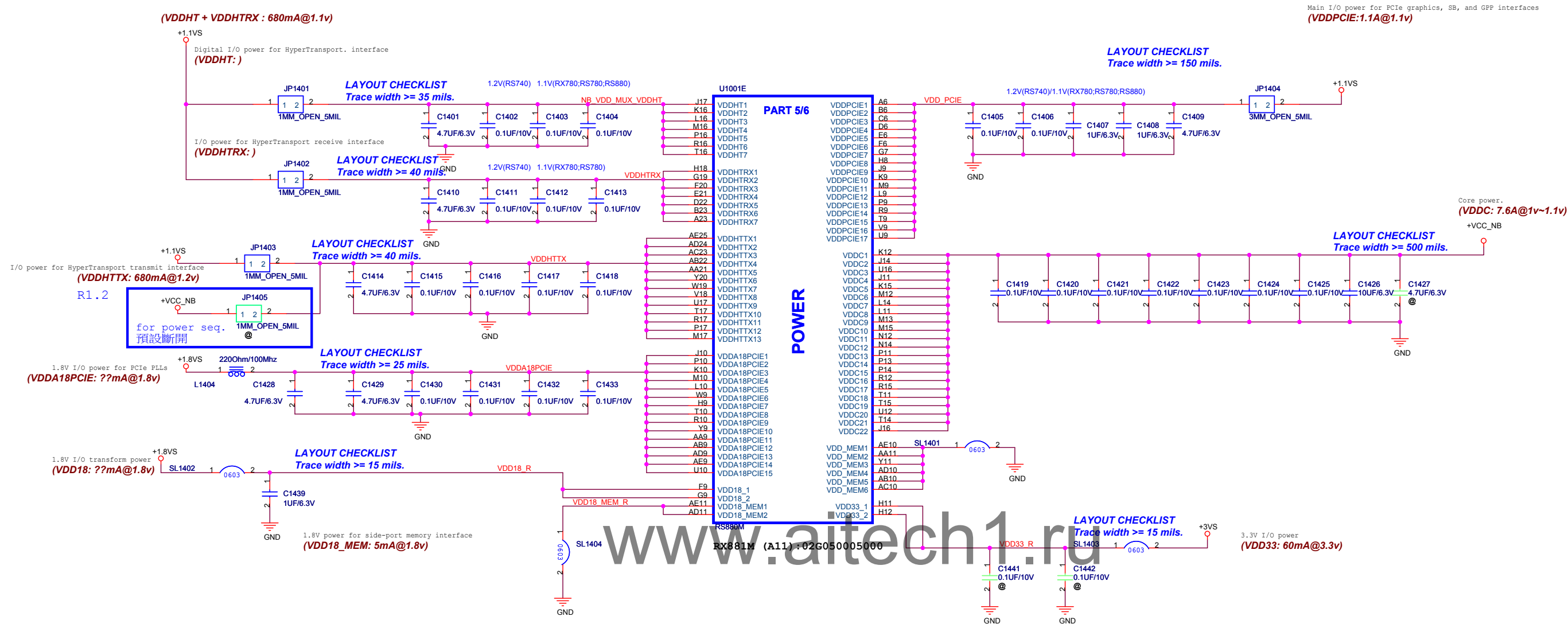
NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

#### R1.1 ITEM5












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		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Uei Lee</i>	
Size <i>A</i>	Project Name <b>N61Da</b>		Rev <i>1.0</i>
Date: <i>Tuesday, March 30, 2010</i>		Sheet <i>15</i> of <i>79</i>	


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		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Uei Lee</i>	
Size <i>A</i>	Project Name <b>N61Da</b>		Rev <i>1.0</i>
Date: <i>Tuesday, March 30, 2010</i>		Sheet <i>16</i> of <i>79</i>	

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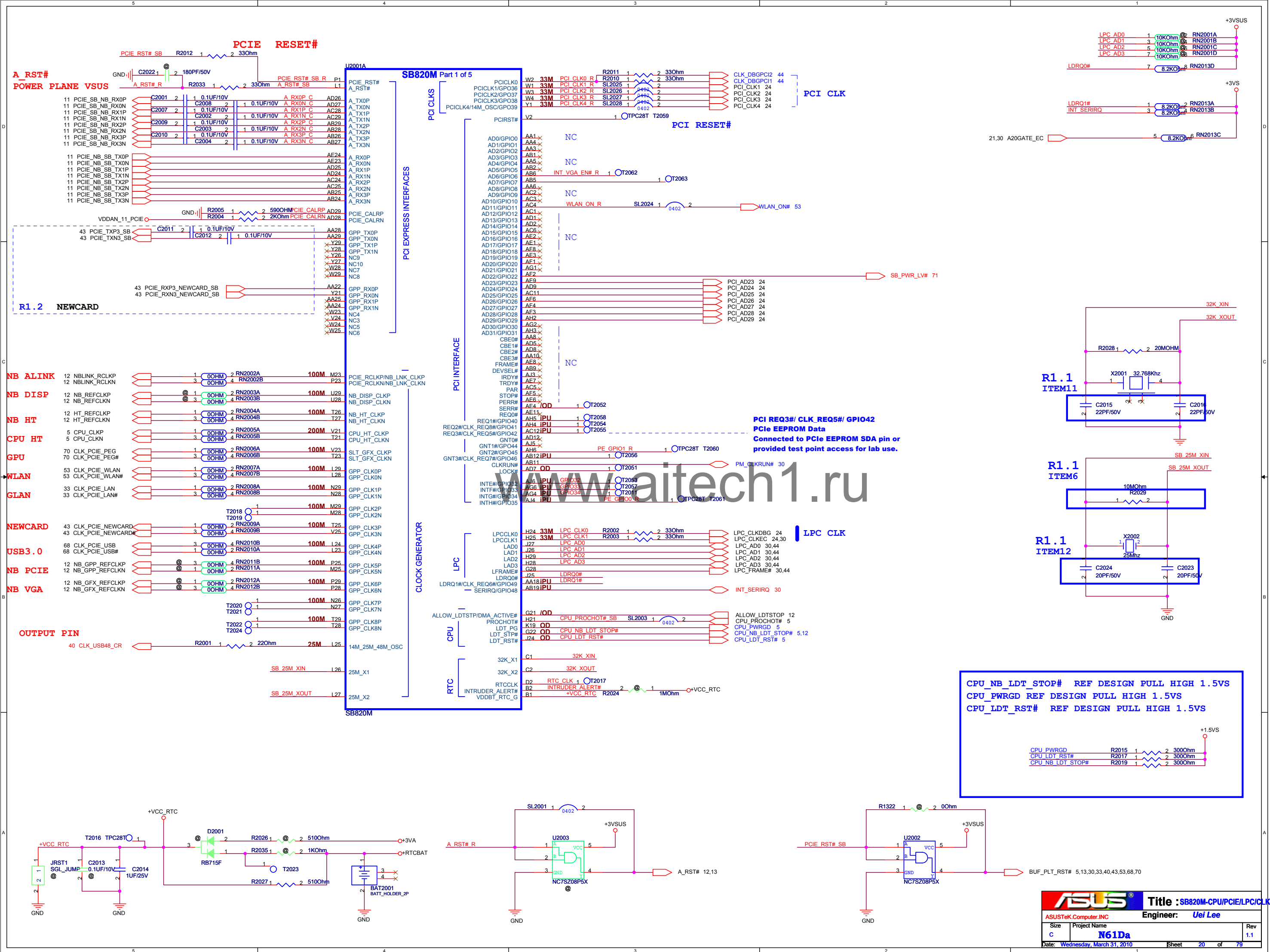
		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Uei Lee</i>	
Size <i>A</i>	Project Name <b>N61Da</b>		Rev <i>1.0</i>
Date: <i>Tuesday, March 30, 2010</i>		Sheet <i>17</i> of <i>79</i>	

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		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Uei Lee</i>	
Size <i>A</i>	Project Name <b>N61Da</b>		Rev <i>1.0</i>
Date: <i>Tuesday, March 30, 2010</i>		Sheet	<i>18</i> of <i>79</i>



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SATA HDD

SATA ODD

ESATA

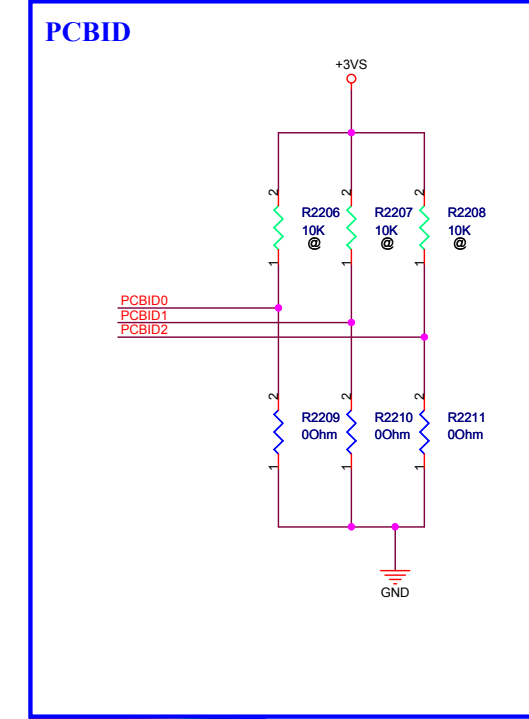
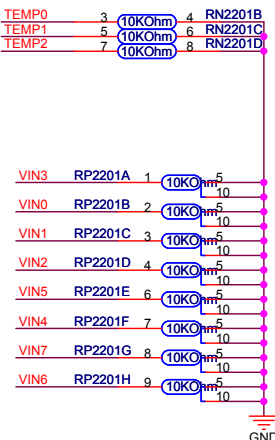
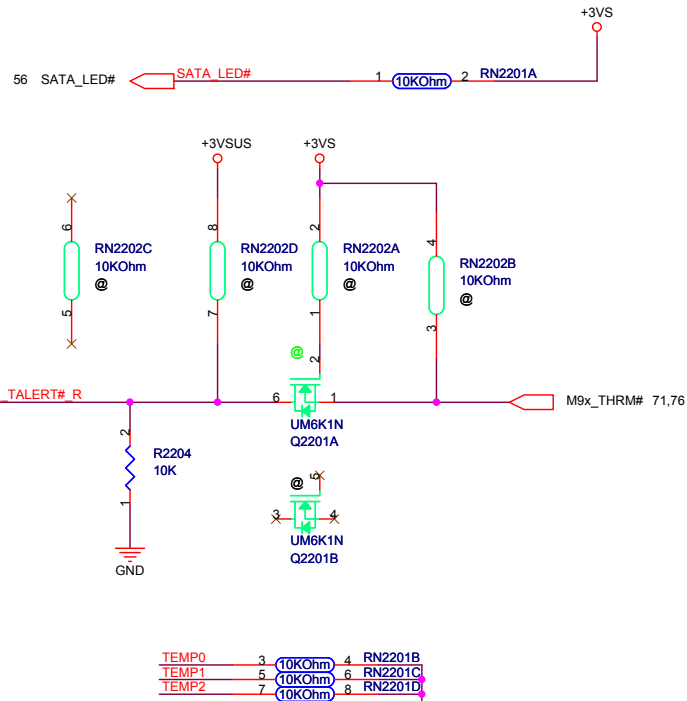
SB820M  
Part 2 of 5

SERIAL ATA

HW MONITOR

SPI ROM

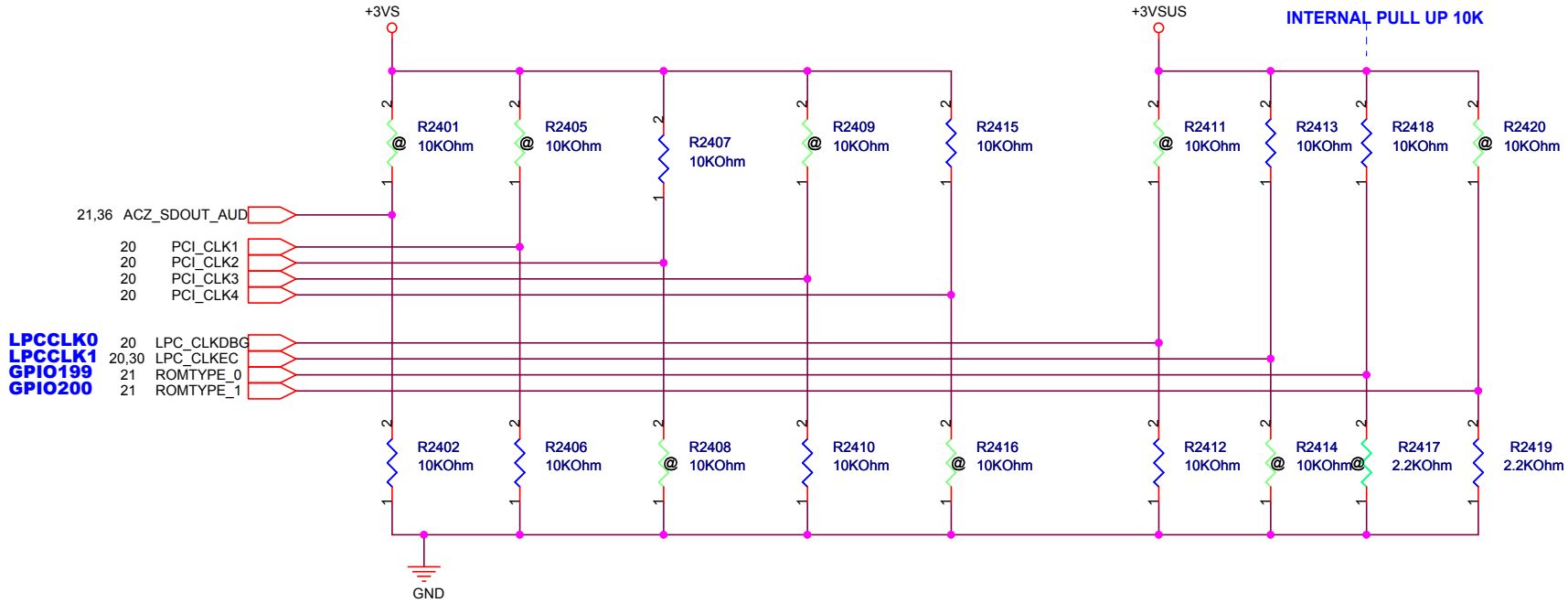
SB710 (A14) :02G050003001





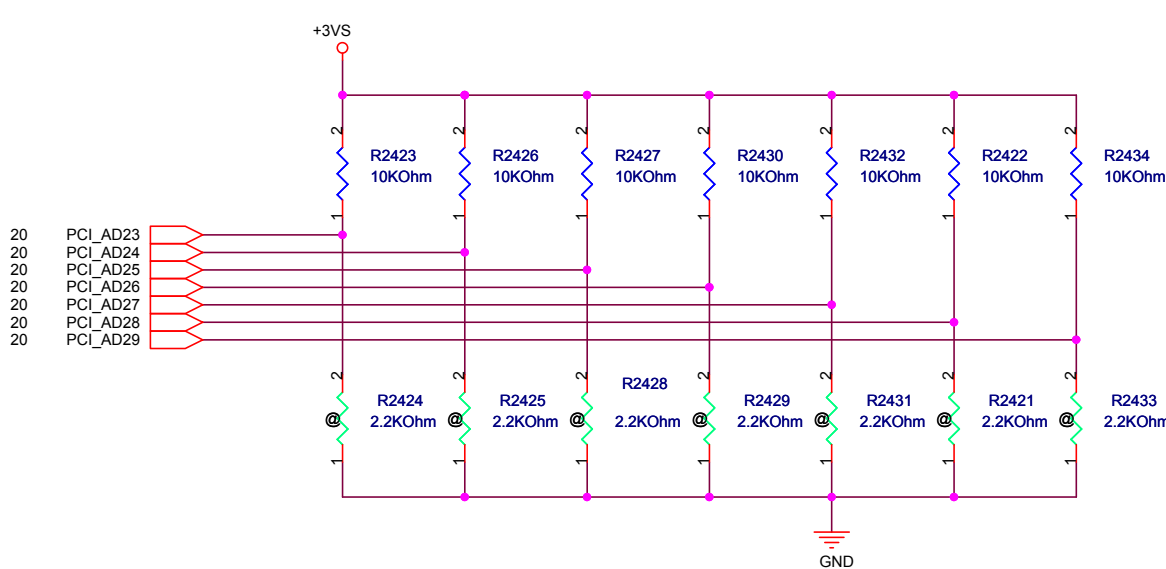






	AZ_SDOUD_AUD	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLKDBG	LPC_CLKEC	ROMTYPE_1	ROMTYPE_0
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enabled DEFAULT	USE DEBUG STRAP	Required setting for integrated clock mode DEFAULT	EC ENABLED	internal CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disabled	IGNORE DEBUG STRAP DEFAULT	Reserved.	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

PCIe Gen Mode  
SB810/SB850:  
Allow PCIe Gen2: 10-k? 5% pull-up to +3.3V\_S0.  
Force PCIe Gen1: 10-k? 5% pull-down.  
SB820M: Only provision for pull-down is required, not installed by default.



	PCI_AD23	PCI_AD24	PCI_AD25	PCI_AD26	PCI_AD27
PULL HIGH	ROMTYPE Strap DEFAULT	Disabled I2C ROM DEFAULT	Use internal PLL FC clock DEFAULT	DISABLE ILA AUTORUN DEFAULT	Use internal PLL clock DEFAULT
PULL LOW	Route ROM fetch to PCI bus	Getting value from I2C EPROM	Bypass internal PLL FC clock	ENABLE ILA AUTORUN	Bypass internal PLL clock

PCI AD27 PCI PLL  
No external resistor (internal pull-up selects PCI PLL).  
Provision for 2.2-k? 5% pull-down (PCI PLL bypassed) or provided test point access for lab use.

PCI AD24 PCIe EEPROM  
No external resistor (internal pull-up selects default PCIe straps).  
Provision for 2.2-k? 5% pull-down (use EEPROM PCIe straps) or provided test point access for lab use.

PCI AD26 ILA AUTORUN  
No external resistor (internal pull-up disables ILA autorun).  
Provision for 2.2-k? 5% pull-down (ILA autorun enabled) or provided test point access for lab use.

PCI AD23 Booting from PCI Memory  
No external resistor(disable booting from PCI memory).  
Provision for 2.2-k? 5% pull-down (enable booting from PCI memory) or provided test point access for lab use.

PCI AD25 FC PLL  
No external resistor (internal pull-up selects FC PLL).  
Provision for 2.2-k? 5% pull-down (FC PLL bypassed) or provided test point access for lab use

5 4 3 2 1


D

C

B


A

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		Title : <b>SM BUS</b>	
ASUSTeK COMPUTER INC. NB3		Engineer: <i>Uei Lee</i>	
Size <b>A</b>	Project Name <b>N61Da</b>		Rev <b>1.1</b>
Date: <b>Tuesday, March 30, 2010</b>		Sheet <b>25</b> of <b>99</b>	

5 4 3 2 1


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		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>ENGINEER</i>	
Size <i>A</i>	Project Name <i>N61Vn</i>		Rev <i>1.0</i>
Date: <i>Tuesday, March 30, 2010</i>		Sheet <i>26</i> of <i>95</i>	

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		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>ENGINEER</i>	
Size <i>A</i>	Project Name <i>N61Vn</i>		Rev <i>1.0</i>
Date: <i>Tuesday, March 30, 2010</i>		Sheet <i>27</i> of <i>95</i>	


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		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>ENGINEER</i>	
Size <i>A</i>	Project Name <i>N61Vn</i>		Rev <i>1.0</i>
Date: <i>Tuesday, March 30, 2010</i>		Sheet <i>28</i> of <i>95</i>	



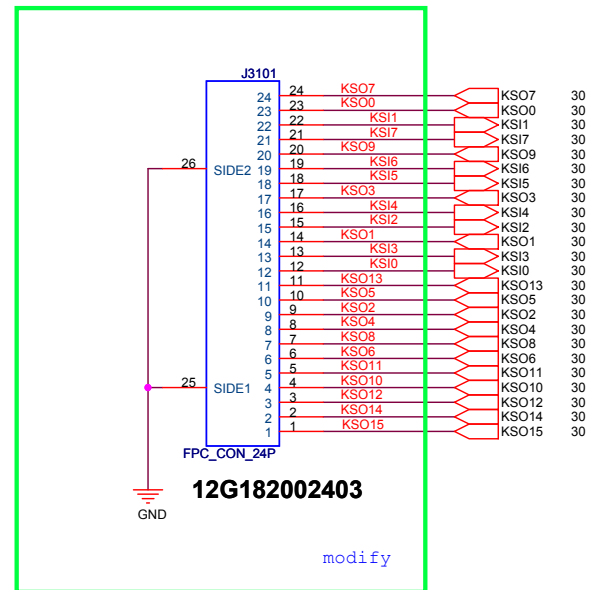
5					4					3					2					1				
D																								
C																								
→																				←				
B																								
A																								

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		Title : <b>CLOCK GEN</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>ENGINEER</b>	
Size <b>A</b>	Project Name <b>N61Da</b>		Rev <b>1.1</b>
Date: <b>Tuesday, March 30, 2010</b>		Sheet <b>29</b> of	<b>95</b>



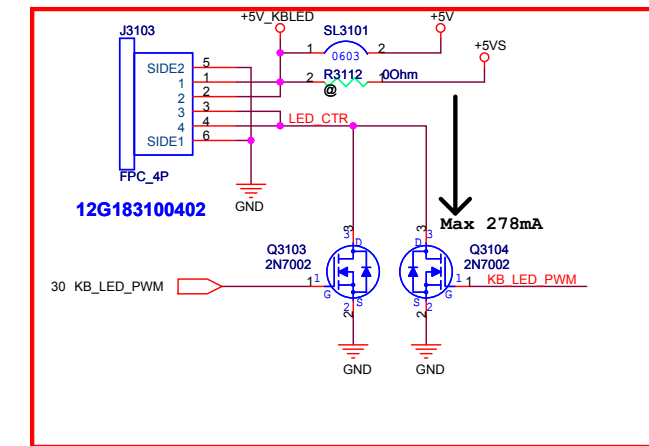
## For Keyboard



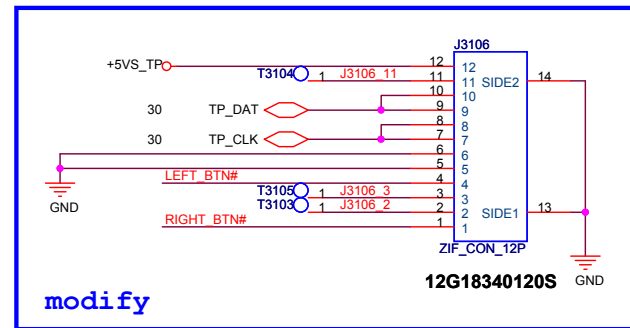
Reserve for EMI

## KB LED

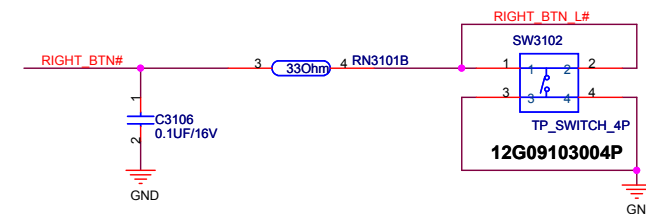
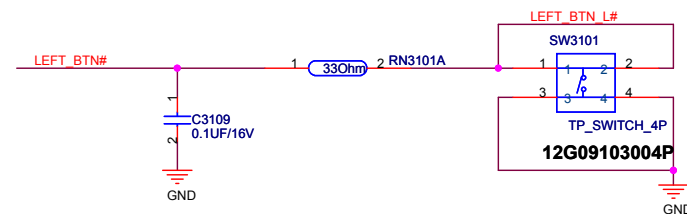
2009/5/18 Add Keyboard LED




## Touchpad Connector



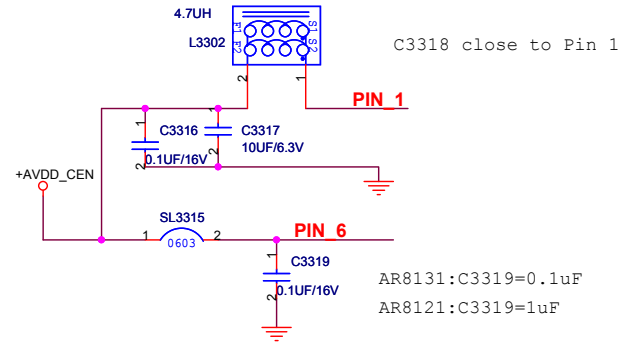
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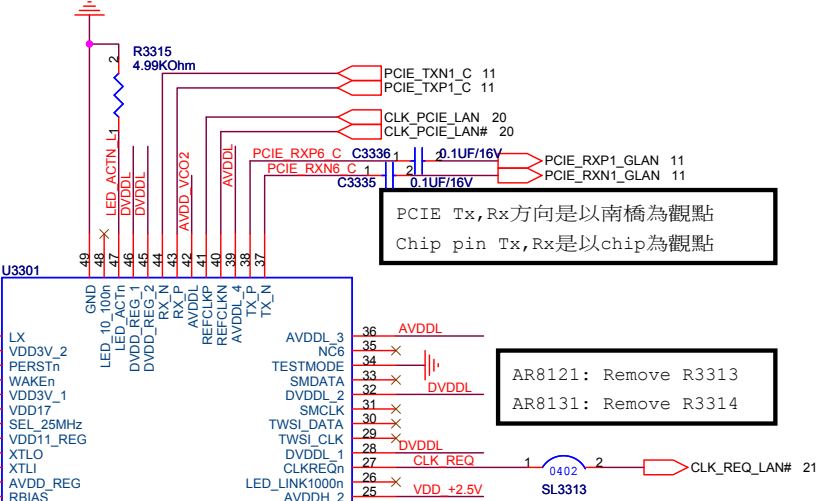
		Title : <b>RST_Reset Circuit</b>	
ASUSTeK COMPUTER INC. NB4		Engineer: <b>UEI LEE</b>	
Size <b>A</b>	Project Name <b>N61JA</b>		Rev <b>1.1</b>
Date: <b>Tuesday, March 30, 2010</b>		Sheet <b>32</b>	of <b>97</b>

AR8131:Remove R3301,C3318  
AR8121:Remove L3302,C3317,R3302



AR8131 with overclock: Remove R3315

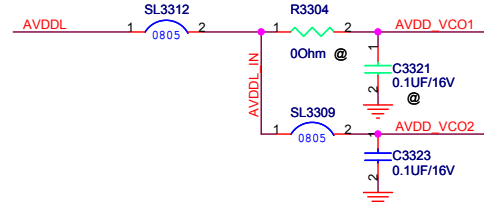
AR8121:Remove R3315



ground pad要打散熱孔

AR8121: Remove R3313  
AR8131: Remove R3314

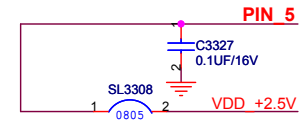
AR8131:Remove L3303  
AR8131:C3321=0.1uF, Remove C3322



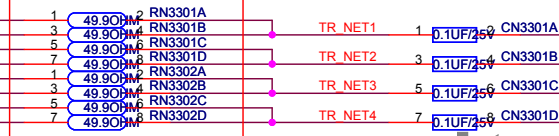
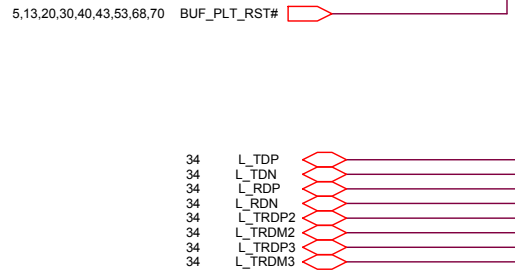
With overclock:Remove R3312  
Not overclock:Remove R3304

AR8131:L3304=0ohm

For AR8131: Remove R3305,R3306,C3324,C3325,C3326,Q3301  
For AR8121: Remove C3327 R3308  
Q3301 close to Pin8

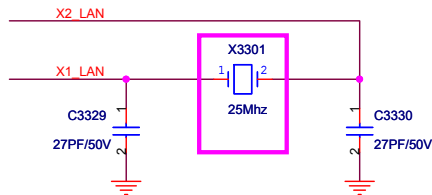


AR8121:Remove R3310  
AR8131/25MHz:Remove R3310 C3333  
AR8131/48MHz:Remove C3333



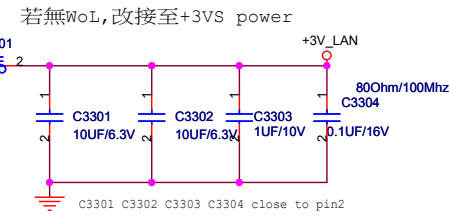
www.aitech1.ru

For AR8131 : Remove R3309

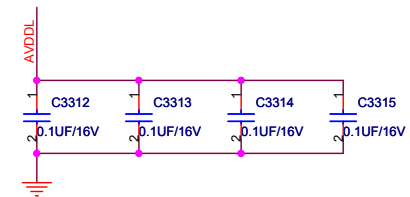
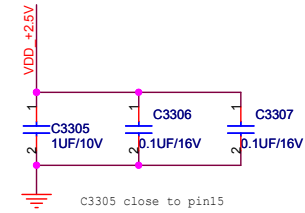


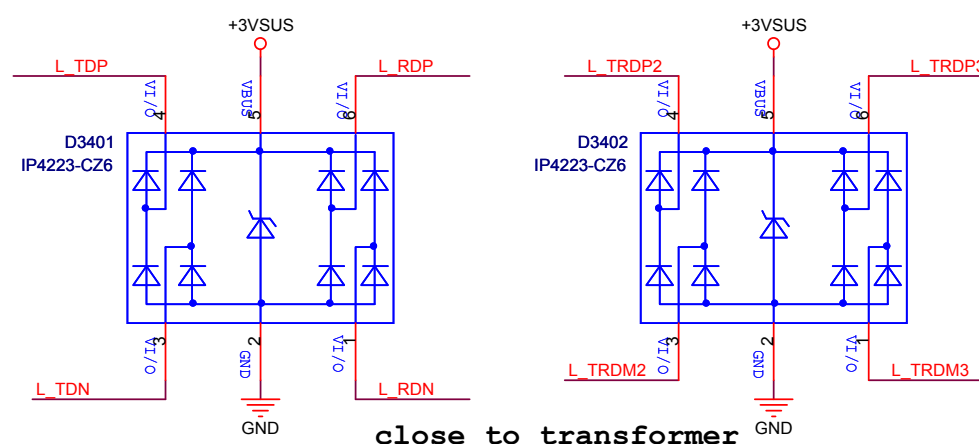
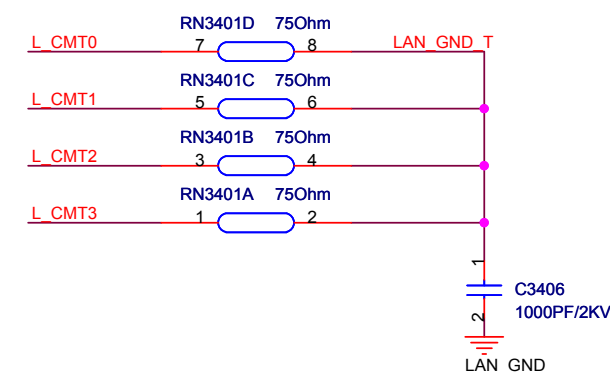
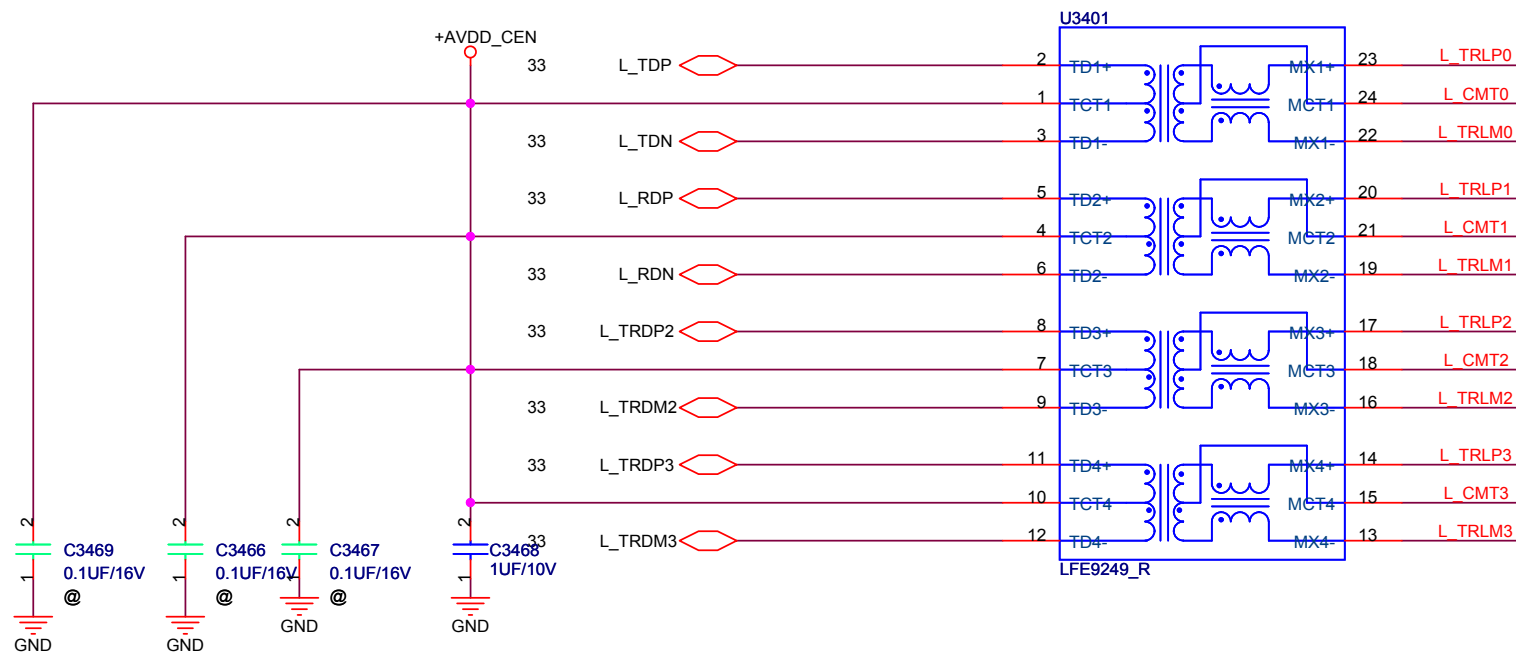
限高問題，換料為 07G010S22500

AR8121:Remove C3328  
AR8131/25MHz: Remove C3328  
AR8131/48MHz: Remove C3329 C3330 X3301

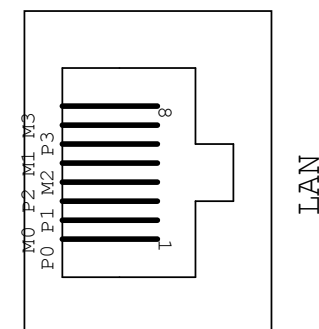
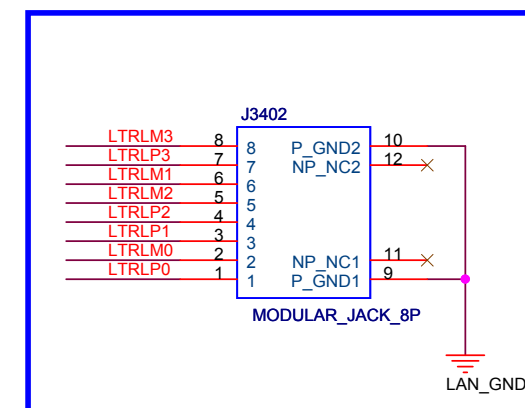
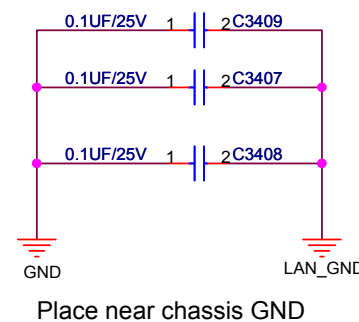


C3308 close to pin45/46






07G001250010 改用 07G028075010 (3/30)

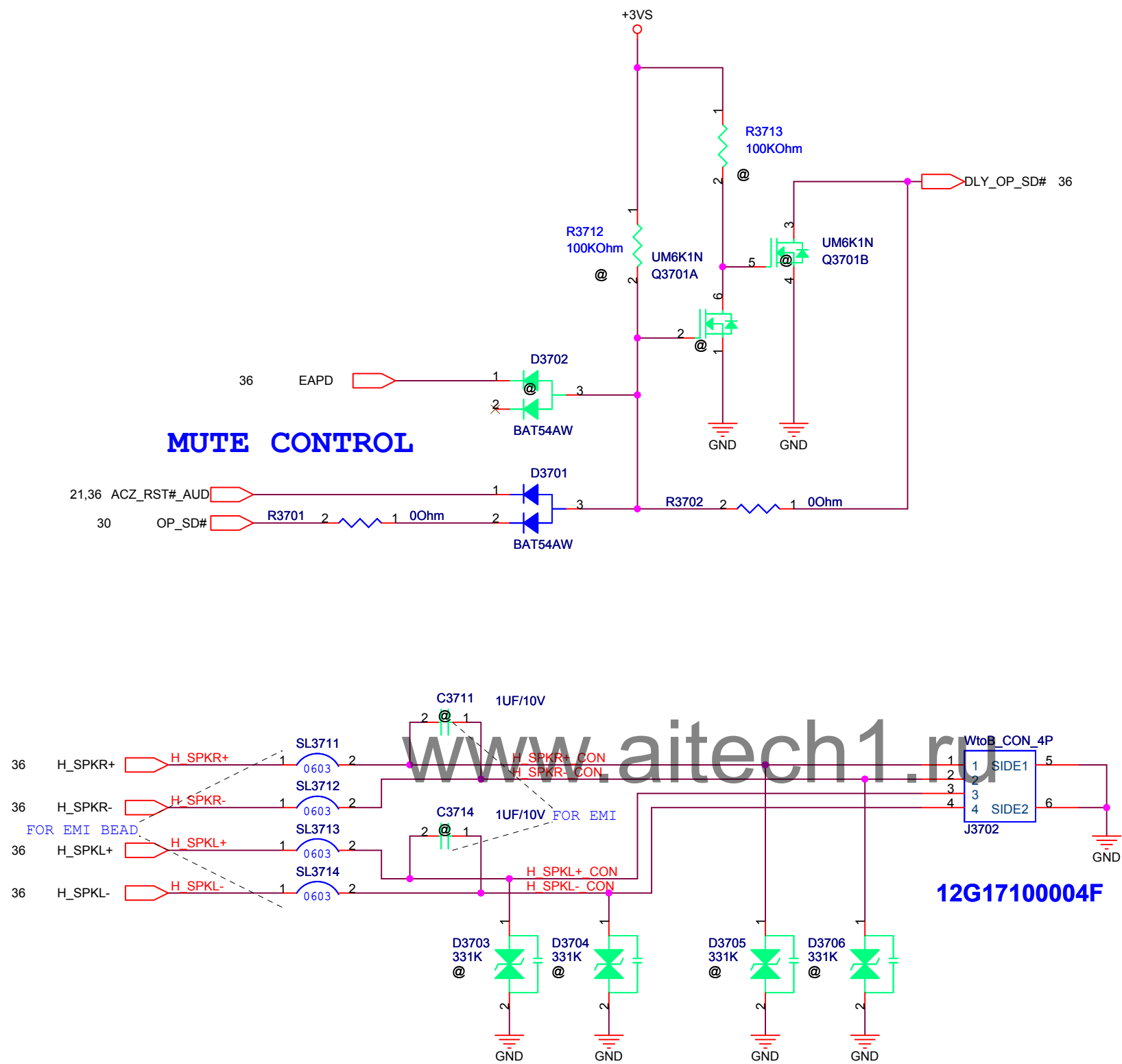


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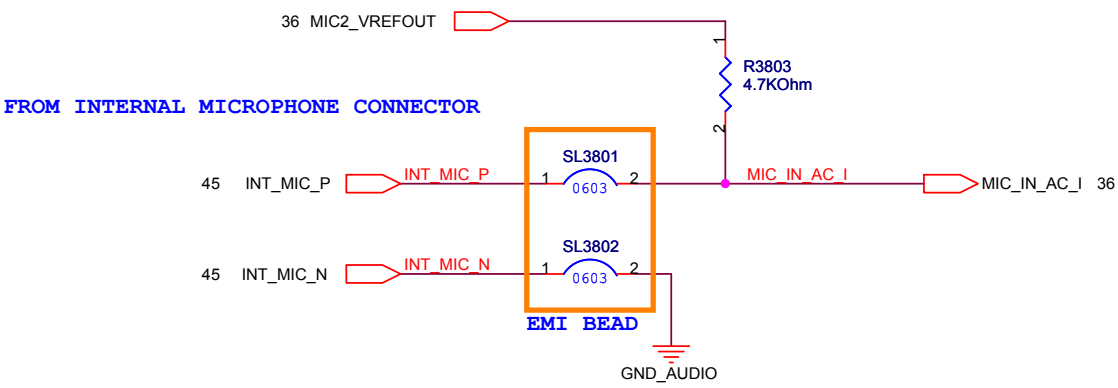
		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: <i>Uei Lee</i>	
Size <i>A</i>	Project Name <b>N61Da</b>		Rev <i>1.1</i>
Date: <i>Tuesday, March 30, 2010</i>		Sheet <i>35</i> of <i>97</i>	



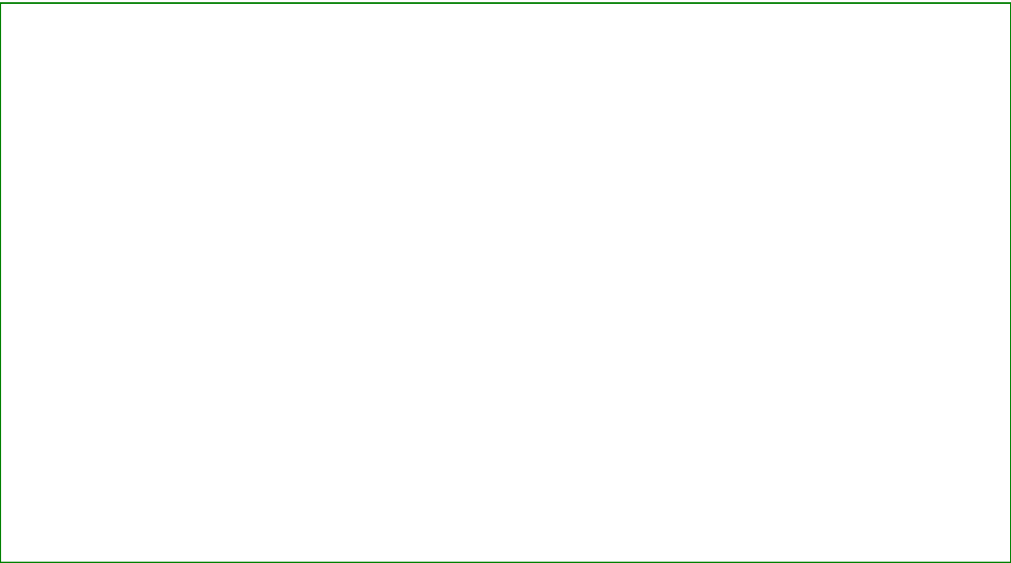




INTERNAL MICROPHONE

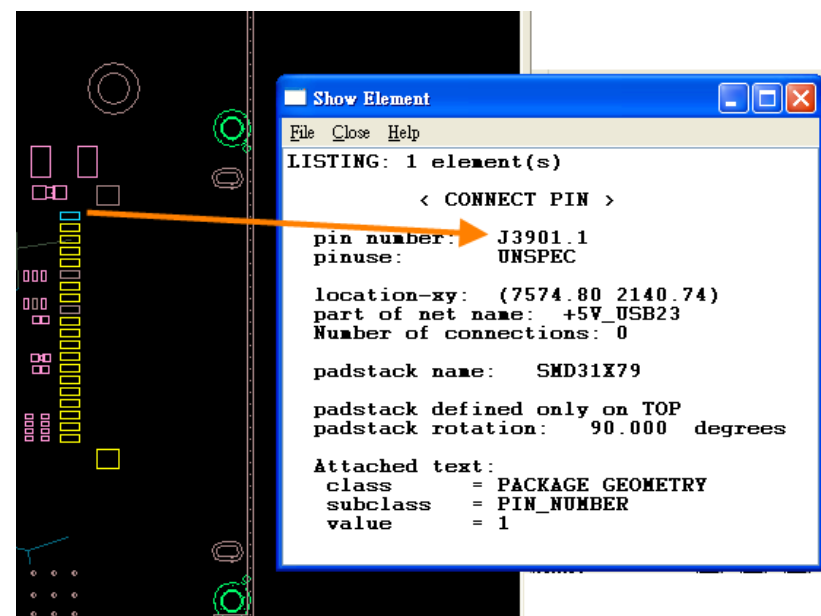
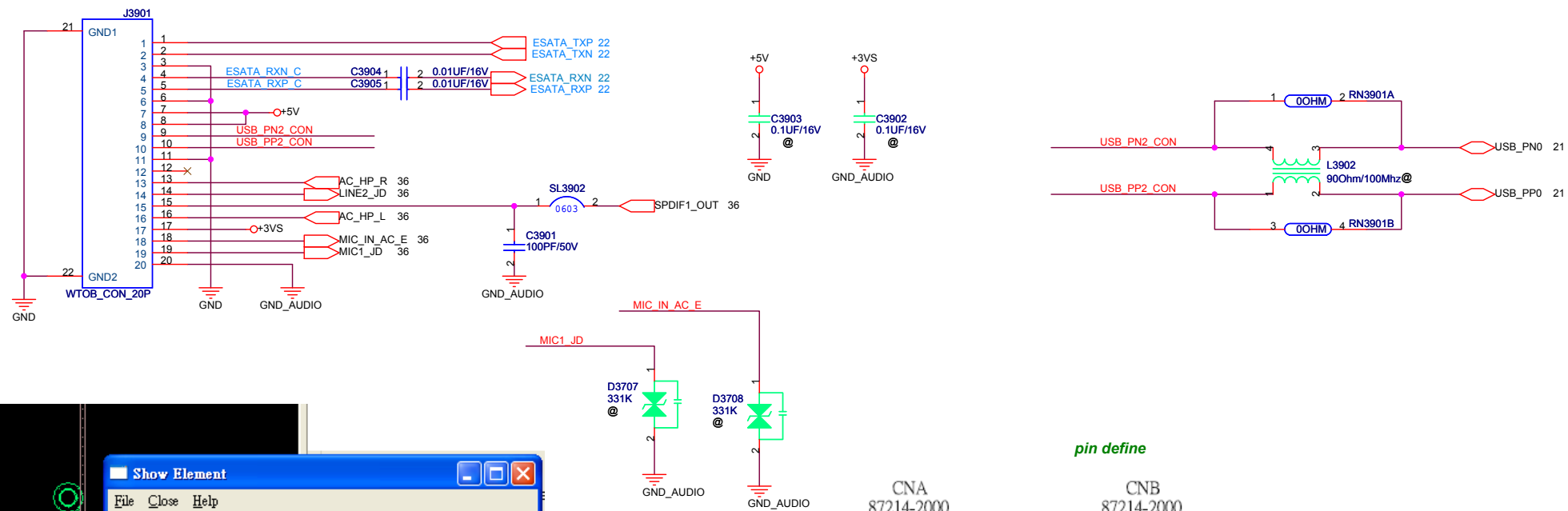


EXTERNAL MICROPHONE



INTERNAL MICROPHONE -- on board

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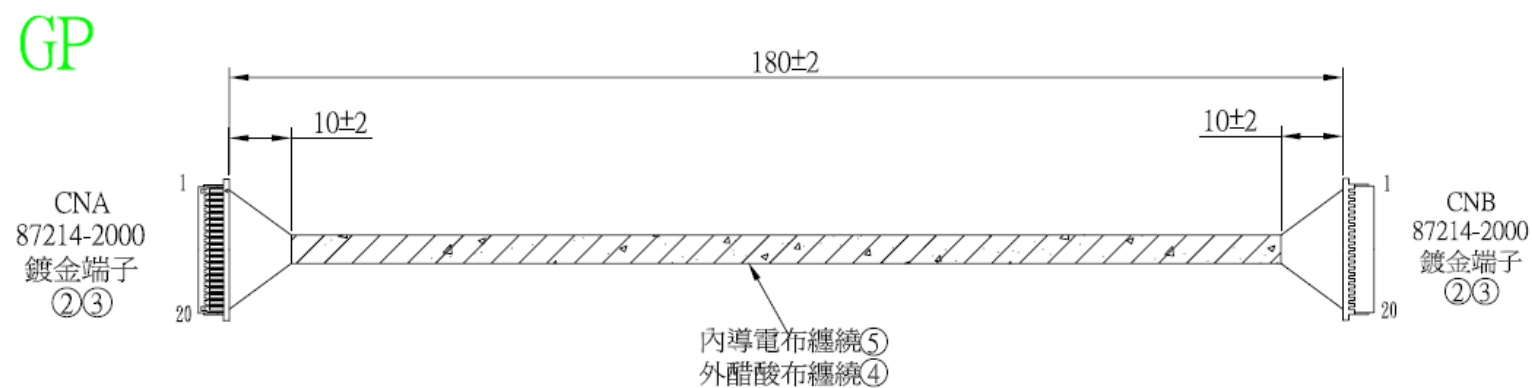


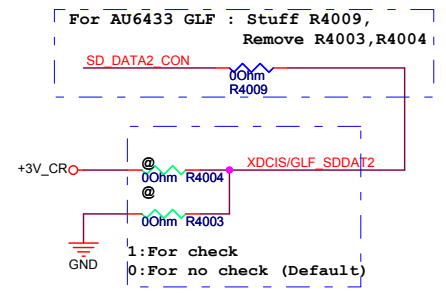
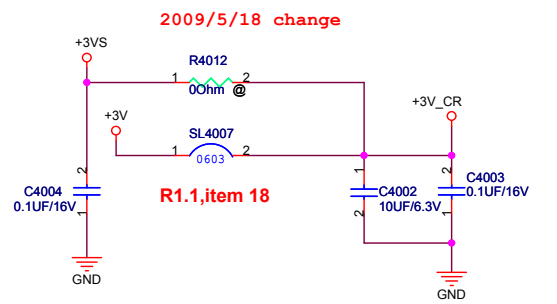
pin define

CNA		CNB
87214-2000		87214-2000
1	紅#32	1
2	白#32	2
3	銅絲#30	3
4	橙#32	4
5	白#32	5
6	銅絲#30	6
7	黑#30	7
8	棕#30	8
9	黃#32	9
10	白#32	10
11	銅絲#30	11
12	紅#32	12
13	橙#32	13
14	黃#32	14
15	綠#32	15
16	藍#30	16
17	紫#32	17
18	灰#32	18
19	白#30	19
20		20

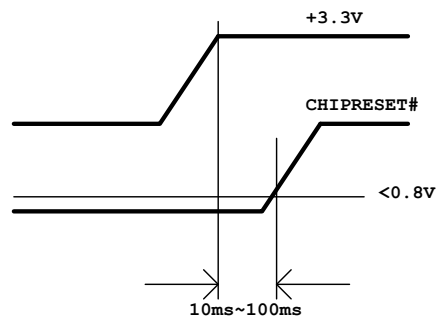
www.altech1.ru

Follow U50 IO cable



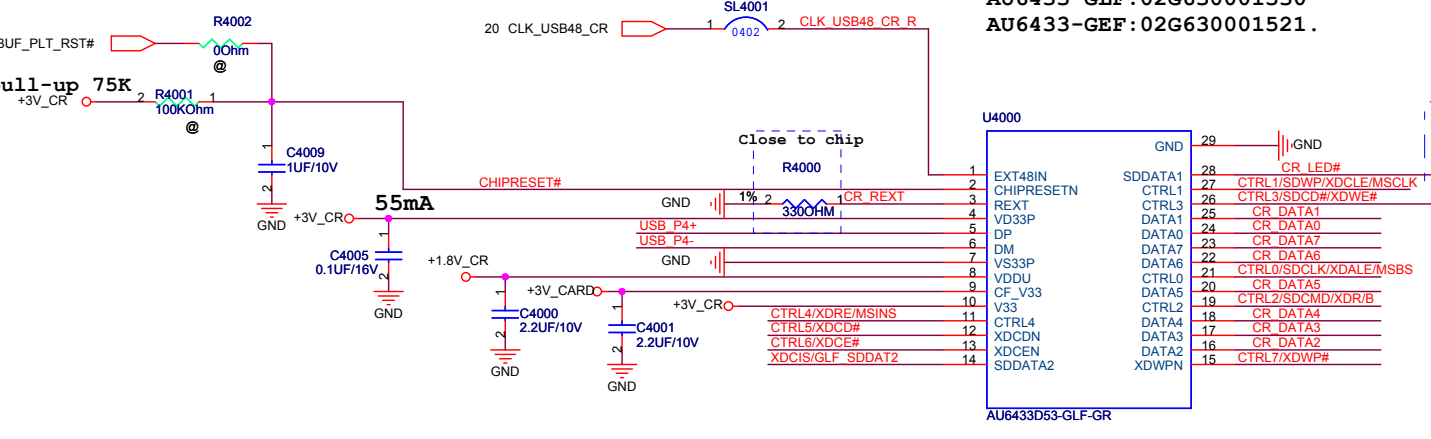


Chip reset Timing:

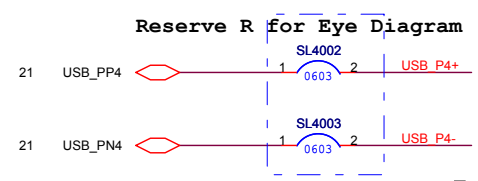
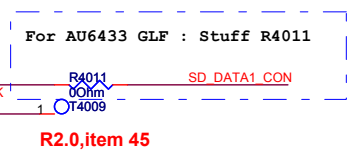


5,13,20,30,33,43,53,68,70 BUF\_PLT\_RST#

Pin2 internal pull-up 75K



AU6433-GLF:02G630001530  
AU6433-GEF:02G630001521.



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xD Pin-assignment

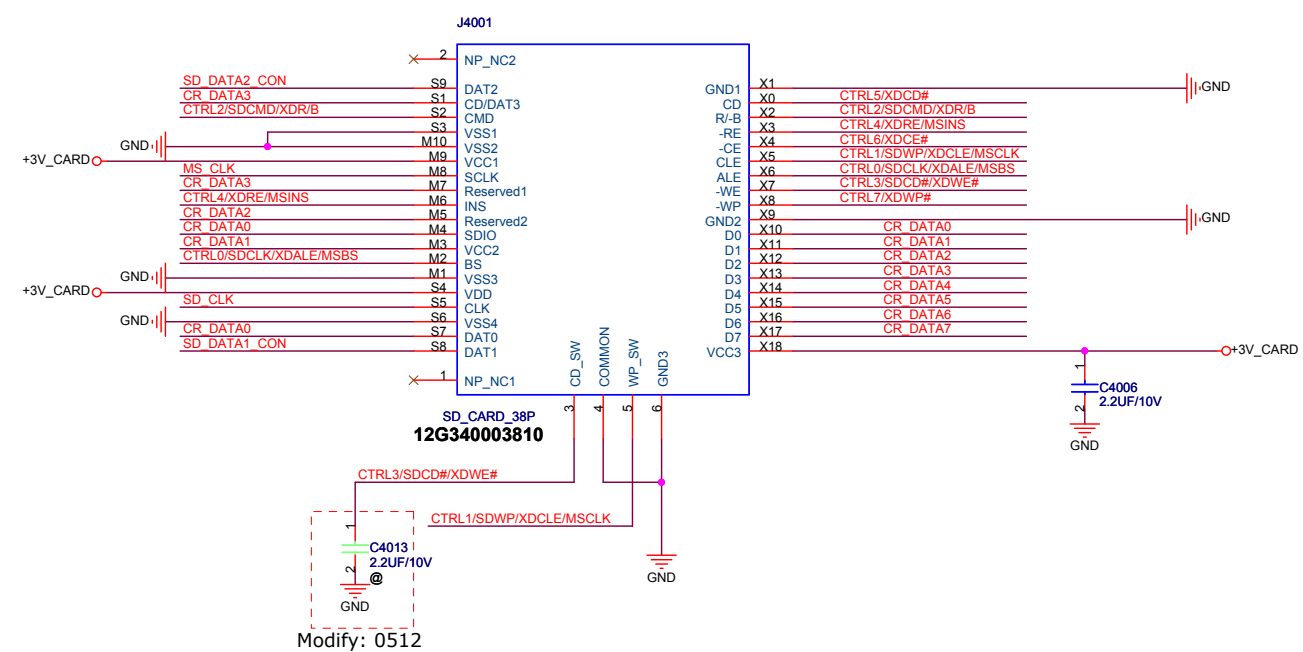
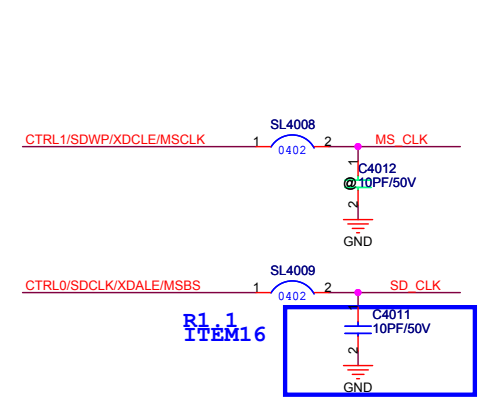
Pin#	PinName
Xd No. 0	CD
Xd No. 1	GND
Xd No. 2	R/-B
Xd No. 3	-RE
Xd No. 4	-CE
Xd No. 5	CLE
Xd No. 6	ALE
Xd No. 7	-WE
Xd No. 8	-WP
Xd No. 9	GND
Xd No.10	D0
Xd No.11	D1
Xd No.12	D2
Xd No.13	D3
Xd No.14	D4
Xd No.15	D5
Xd No.16	D6
Xd No.17	D7
Xd No.18	VCC

MS Pin-assignment

Pin#	PinName
MS No. 1	GND
MS No. 2	BS
MS No. 3	DATA1
MS No. 4	SDIO/DATA0
MS No. 5	DATA2
MS No. 6	INS
MS No. 7	DATA3
MS No. 8	SCLK
MS No. 9	VCC
MS No.10	GND

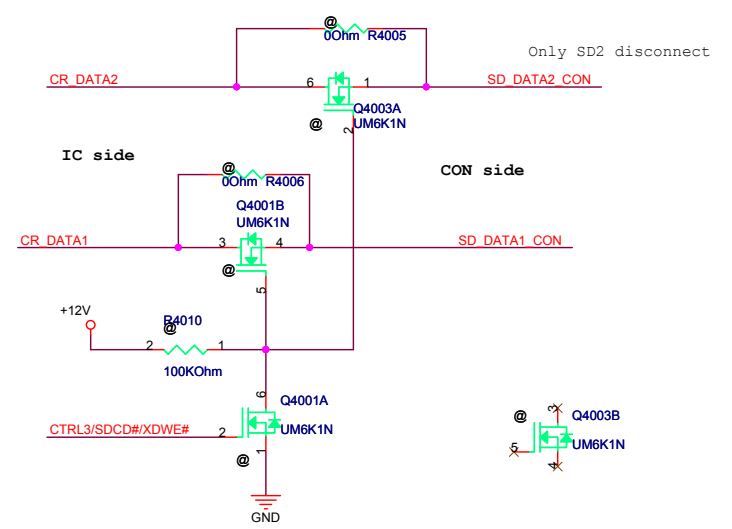
SD Pin-assignment

Pin#	PinName
SD No. 1	CD/DATA3
SD No. 2	CMD
SD No. 3	GND
SD No. 4	VDD
SD No. 5	CLK
SD No. 6	GND
SD No. 7	DATA0
SD No. 8	DATA1
SD No. 9	DATA2



Fix MS Duo Adaptor short issue.  
(SD\_DAT1, SD\_DAT2, XD\_GND short, XD\_CD# may be possible short)


For AU6433-GLF: No stuff All  
For AU6433-GEF: Stuff Q4000, Q4001, Q4003, R4010



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Title : CB\_\*\*\*\*

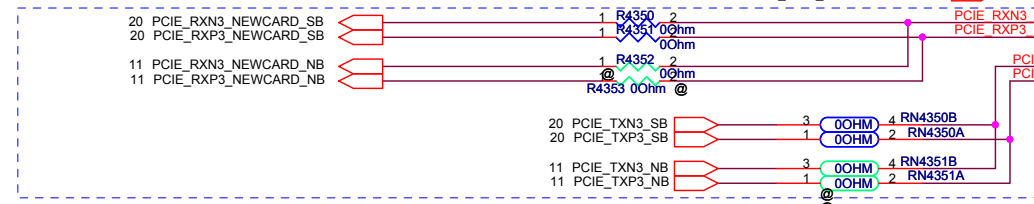
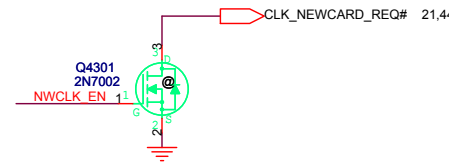
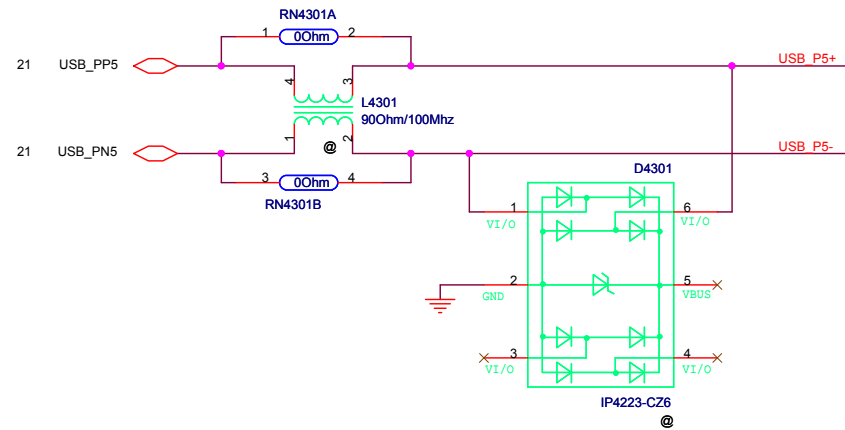
ASUSTeK COMPUTER INC. NB4

Engineer: Uei Lee

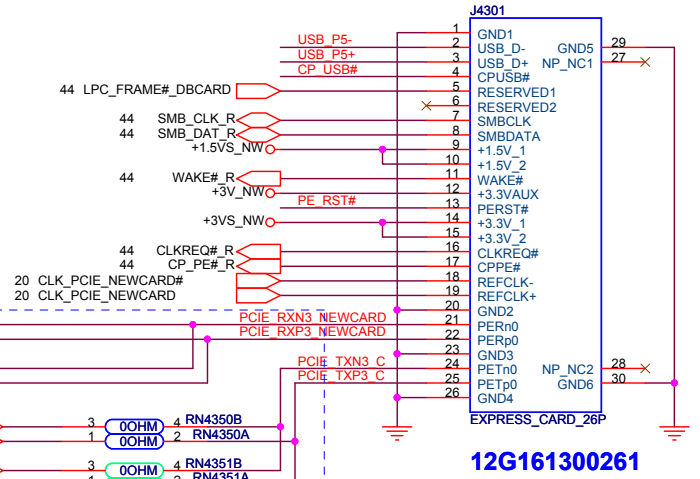
Size B	Project Name N61Da	Rev 1.0
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Date: Tuesday, March 30, 2010Sheet 42 of 97

# Main Board



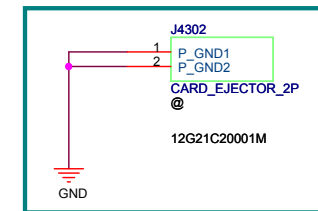
## NewCard Header



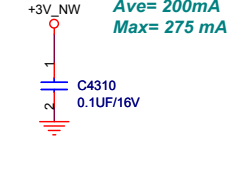
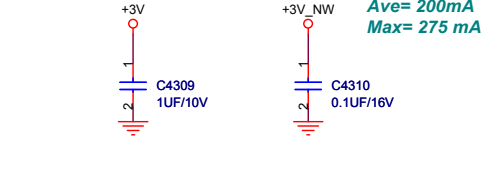
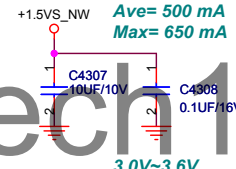
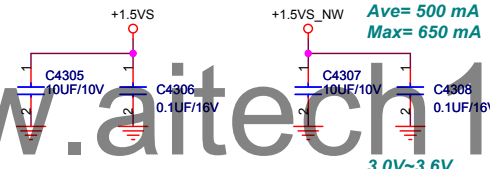
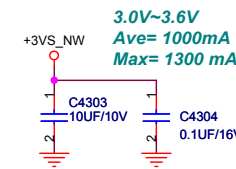
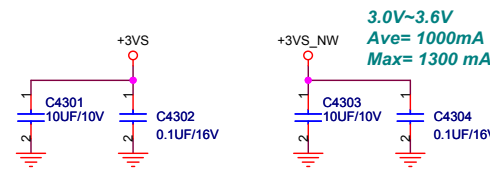
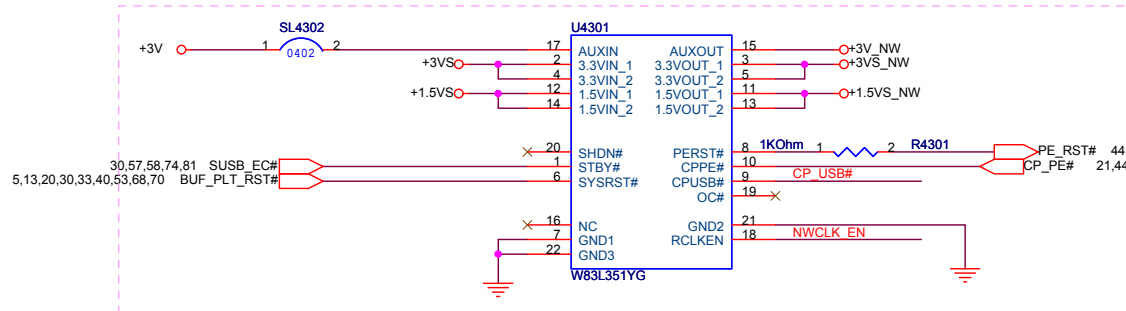
12G161300261

R1.2 與SB colay , 預設接至SB , 電阻靠近分支處

## NewCard Ejecter

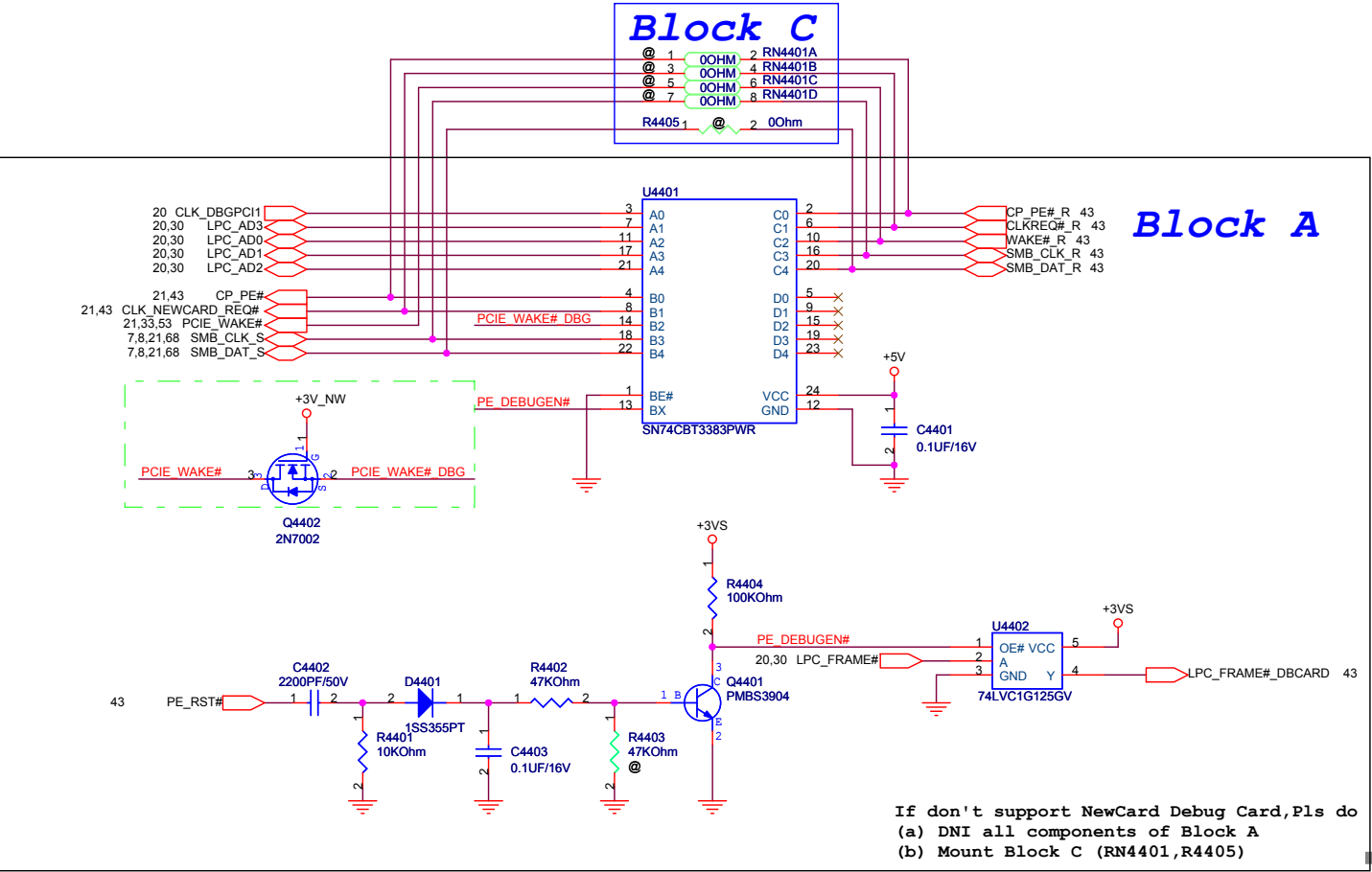


If AUXIN use +3VSUS.  
It would leakage from AUXIN to STBY,SHDN#,PERST#.

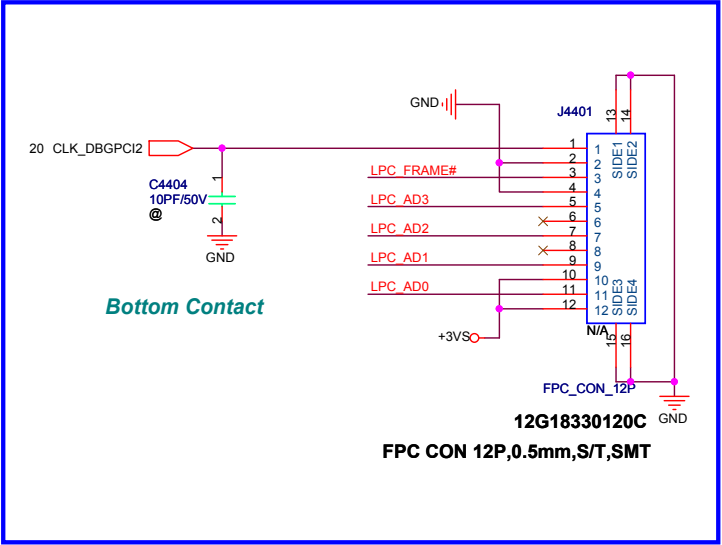


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For NewCard Debug Card



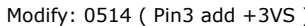
LPC Debug Port



Bottom Contact

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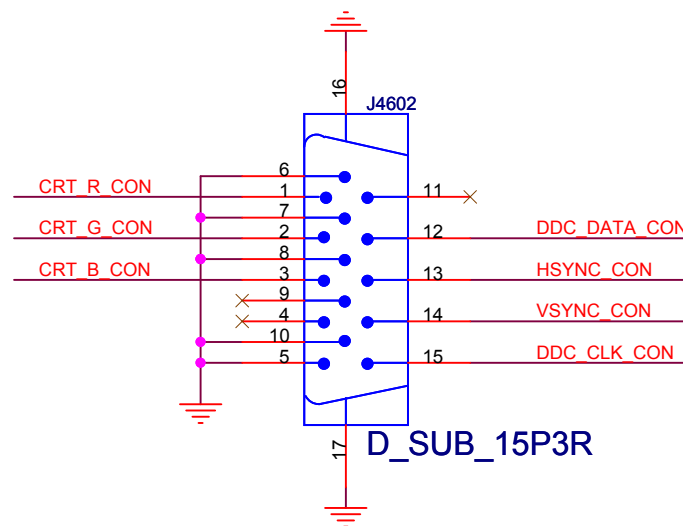
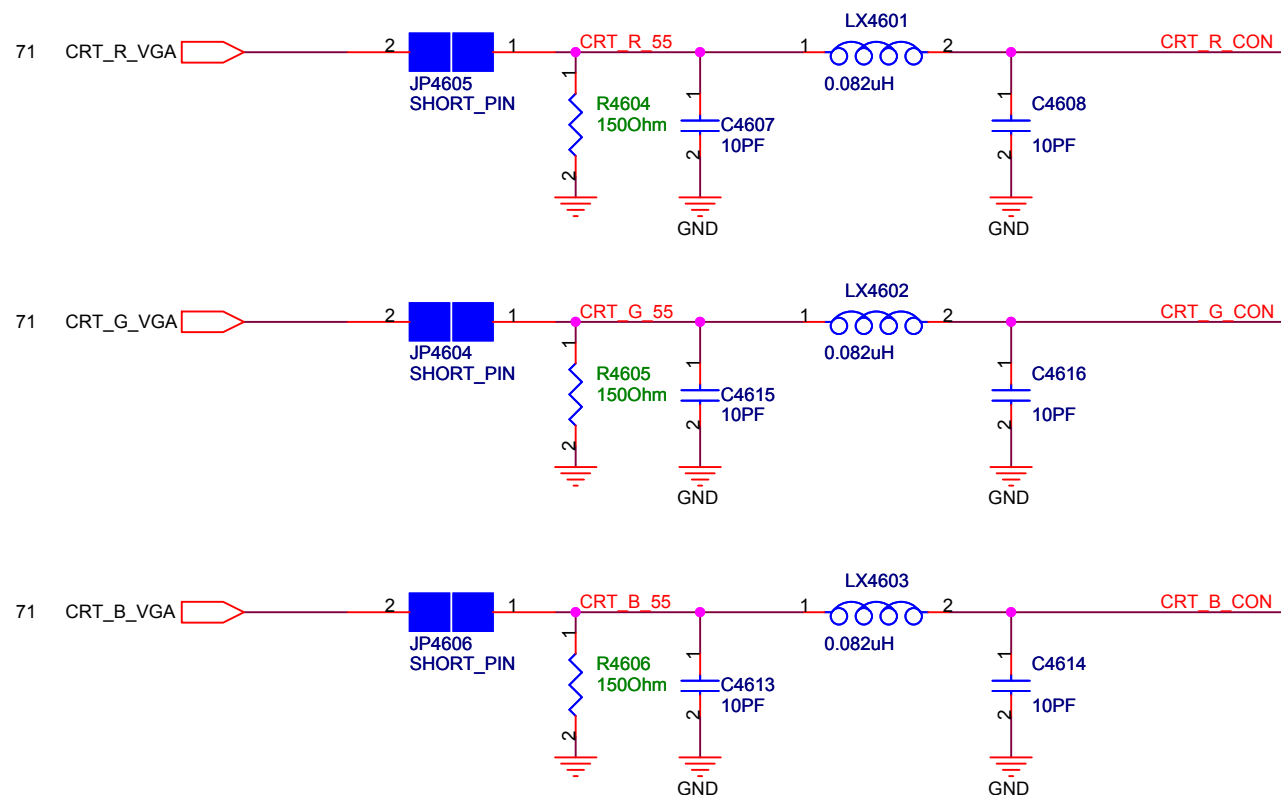
## LCD Power



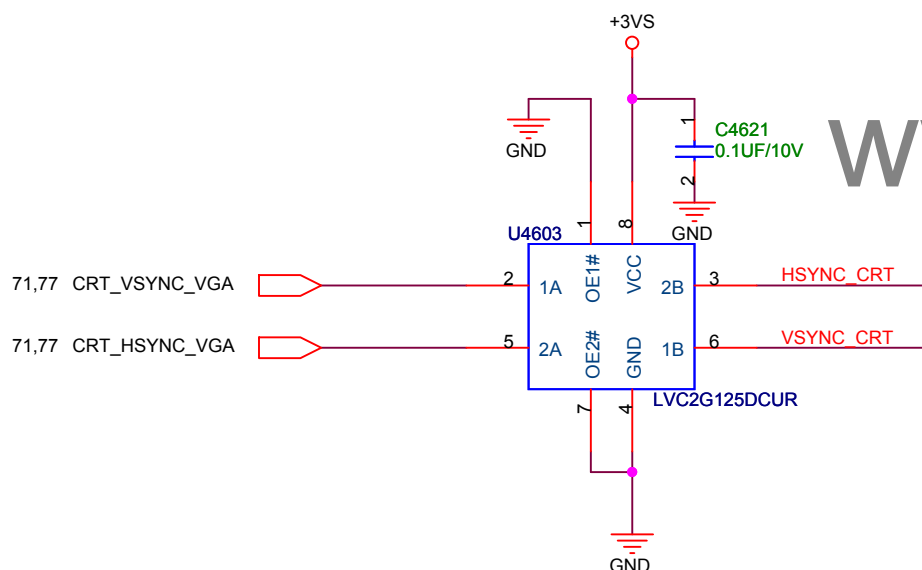
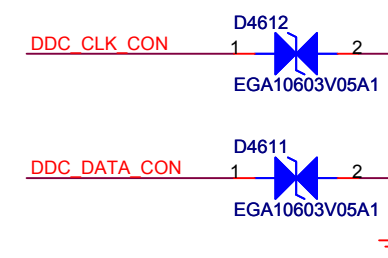
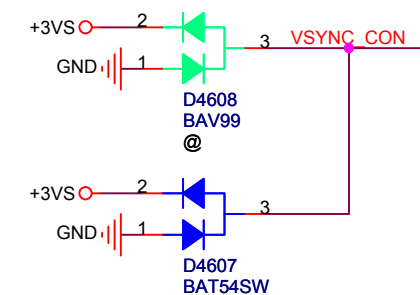
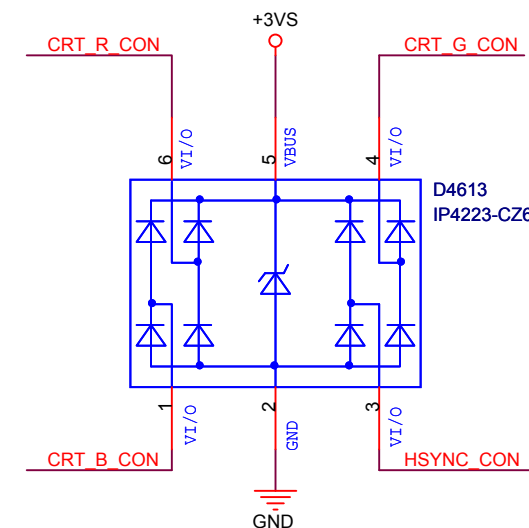
```
check BL EN high
```



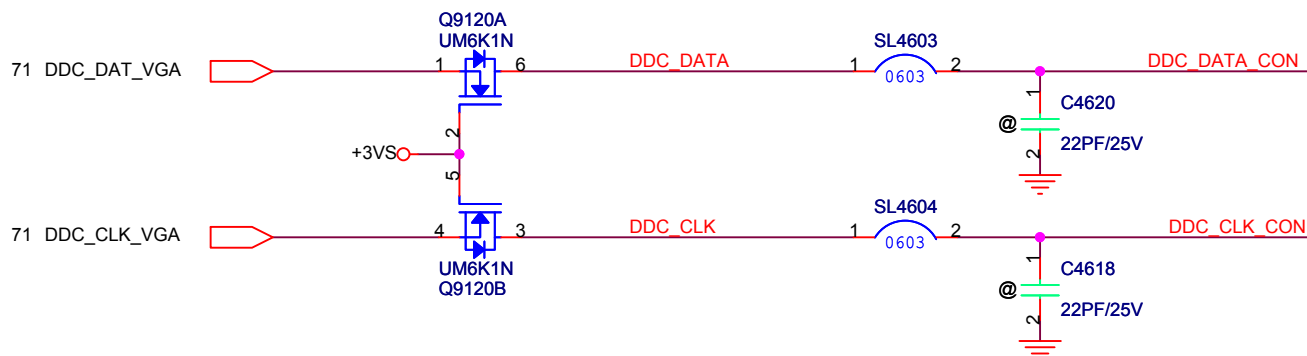
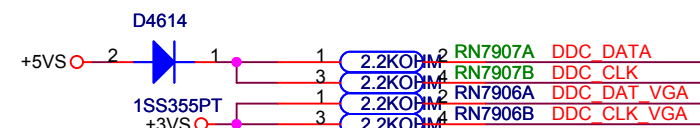
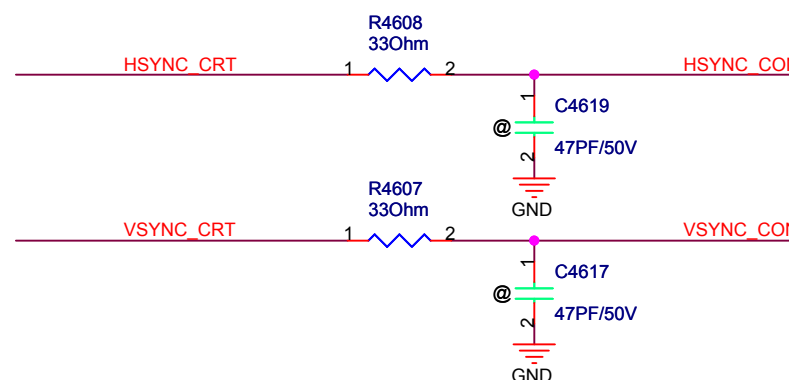
# Main Board



PLACE ESD Diodes near connector




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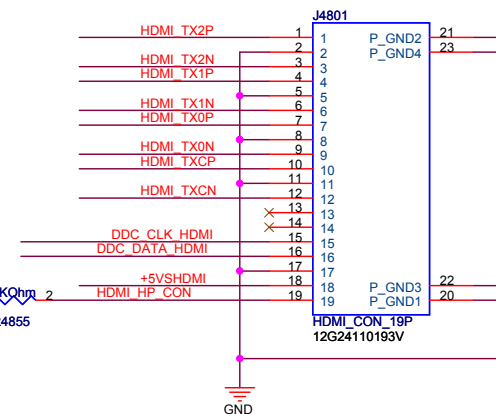
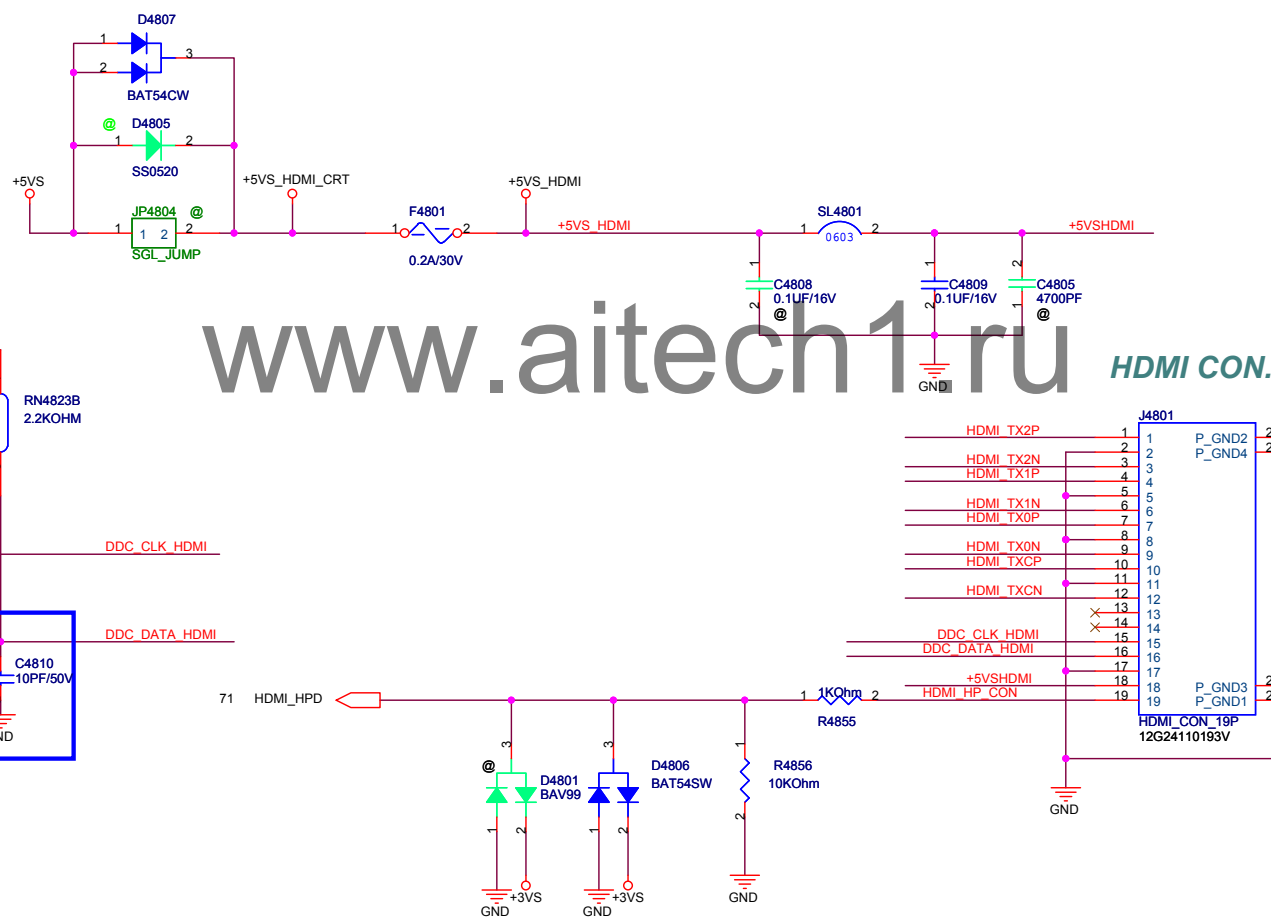
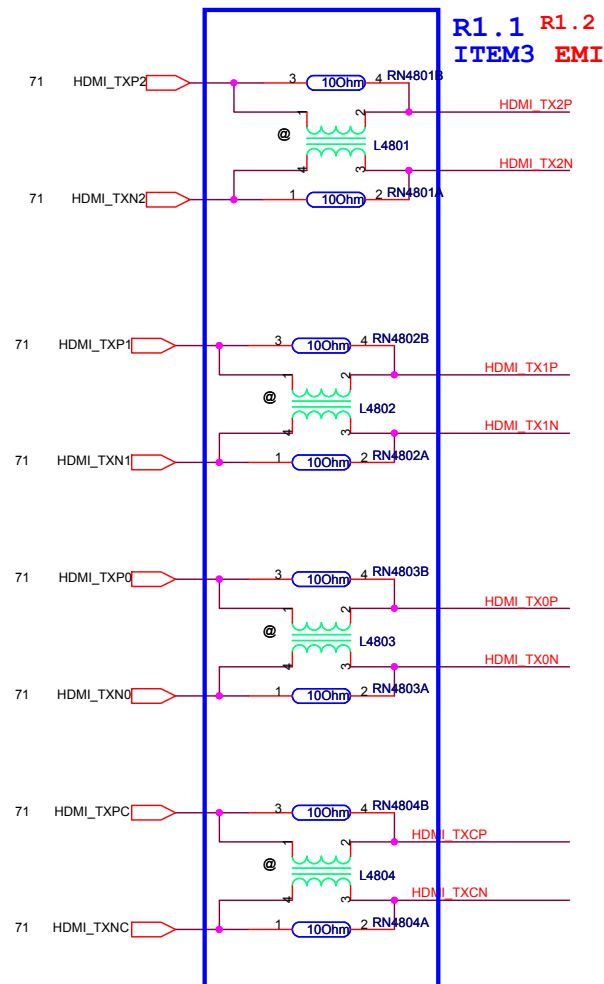
<b>ASUS</b>		Title : CRT_D-Sub	
ASUSTeK COMPUTER INC. NB4		Engineer: Uei Lee	
Size B	Project Name N61Da		Rev 1.1
Date: Wednesday, March 31, 2010		Sheet 46 of 97	

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		Title : <b>Display Port</b>	
ASUSTeK COMPUTER INC. NB4		Engineer: <b>Uei Lee</b>	
Size <b>A</b>	Project Name <b>N61Da</b>		Rev <b>1.1</b>
Date: <b>Tuesday, March 30, 2010</b>		Sheet <b>47</b> of <b>97</b>	




Close to CONNECTOR



R1.2 EMI

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		Title : TV_***	
ASUSTeK COMPUTER INC. NB4		Engineer: Uei Lee	
Size B	Project Name N61Da		Rev 1.1
Date: Tuesday, March 30, 2010		Sheet	49 of 97

Thermal Sensor

1st source: 06G023096010

2nd source: 06G023026012

TEMP.SENSOR G780P11U SOP-8

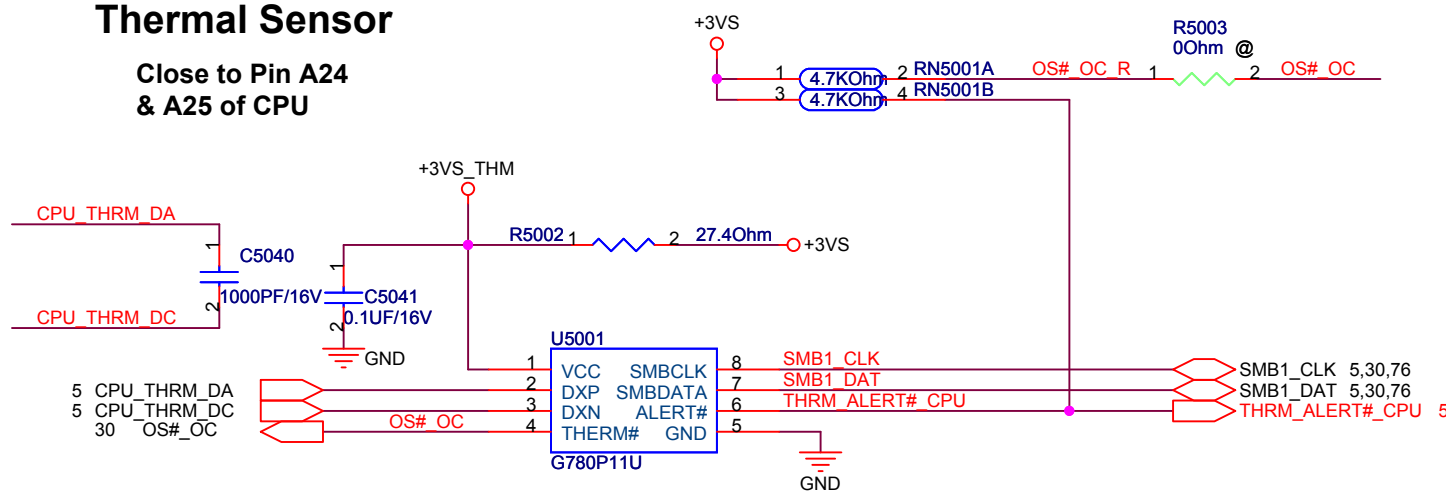
TEMP SENSOR MAX6657YMS+ SOP-8

GMT

MAXIM

Thermal Sensor

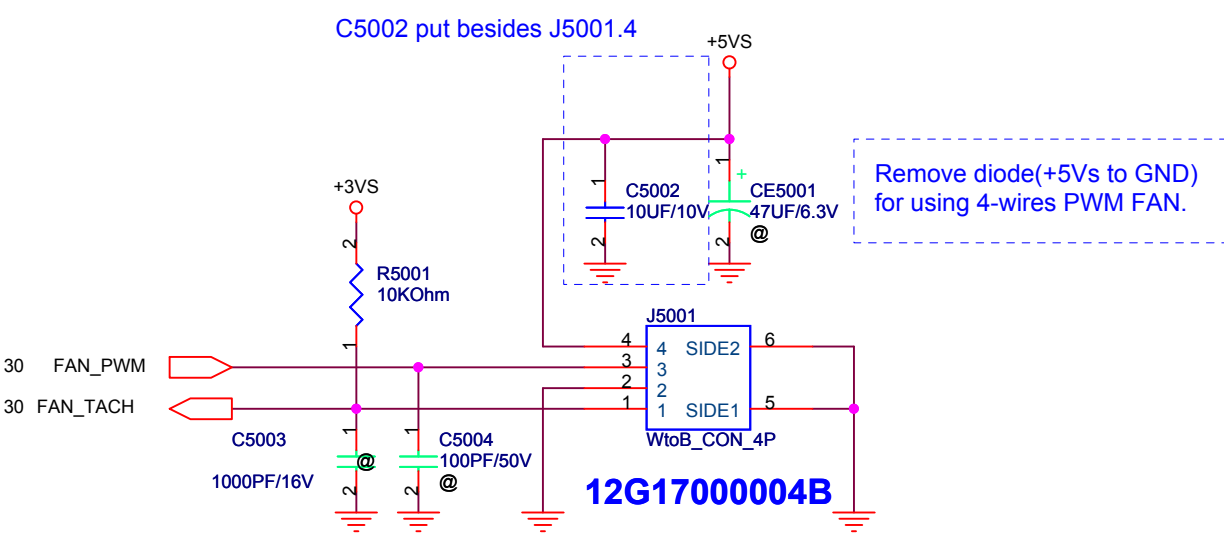
Close to Pin A24  
& A25 of CPU



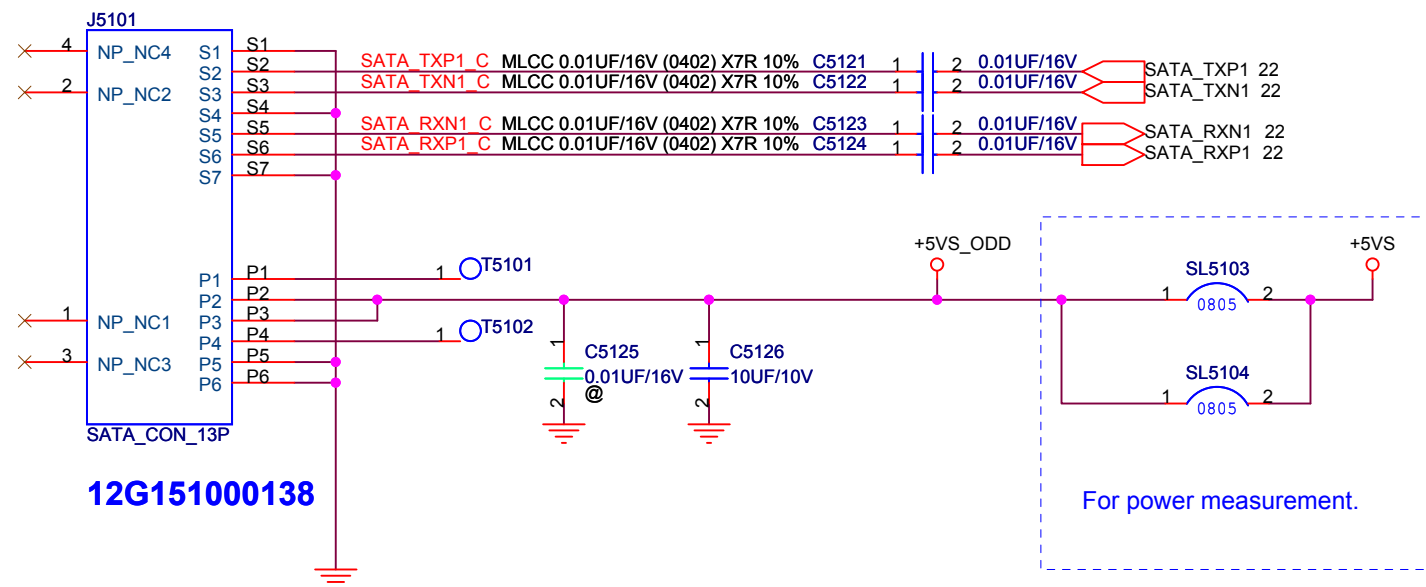
Slave address: 98h

www.aitech1.ru

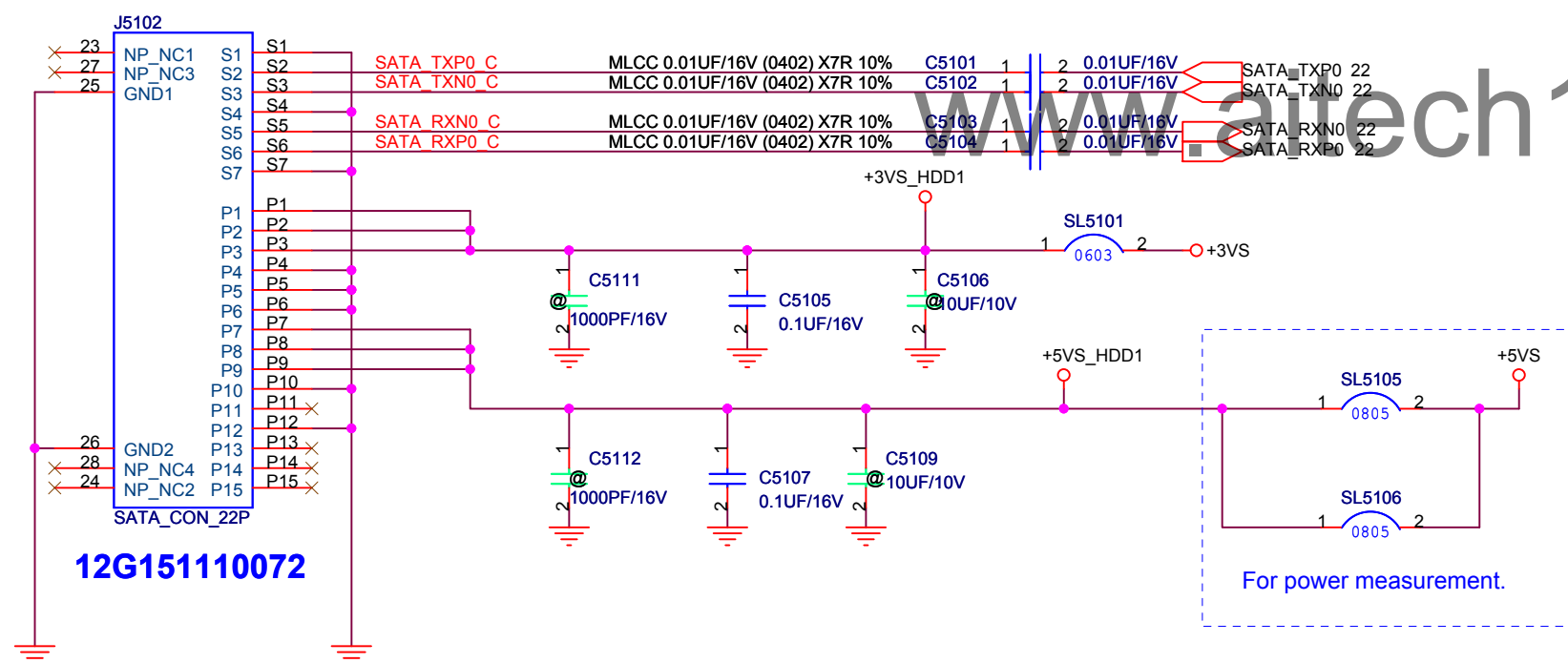
PWM Fan



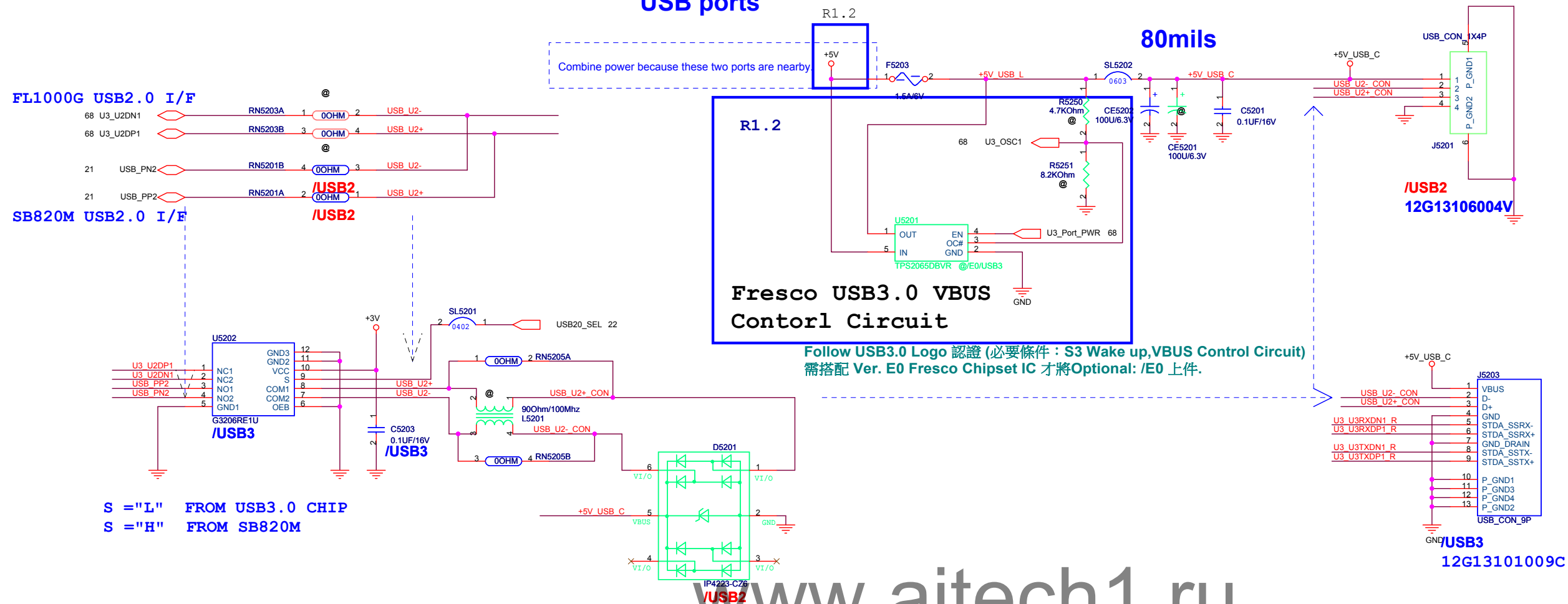
## ODD



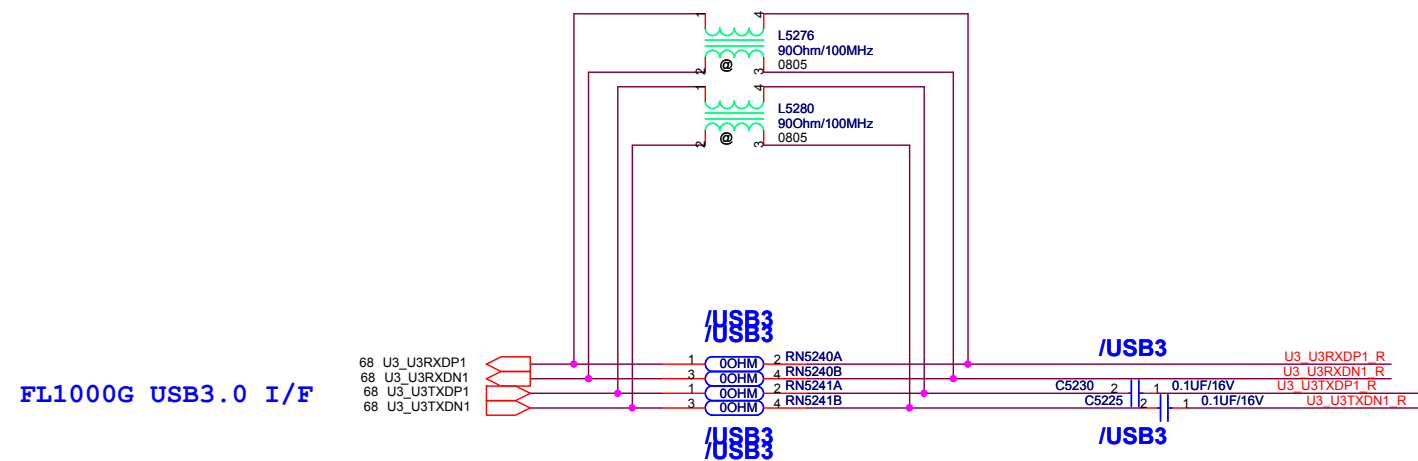
## HDD



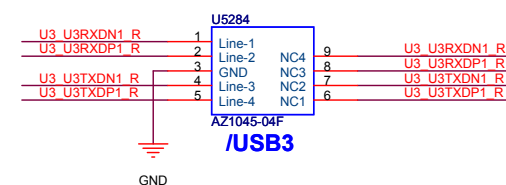
## USB ports



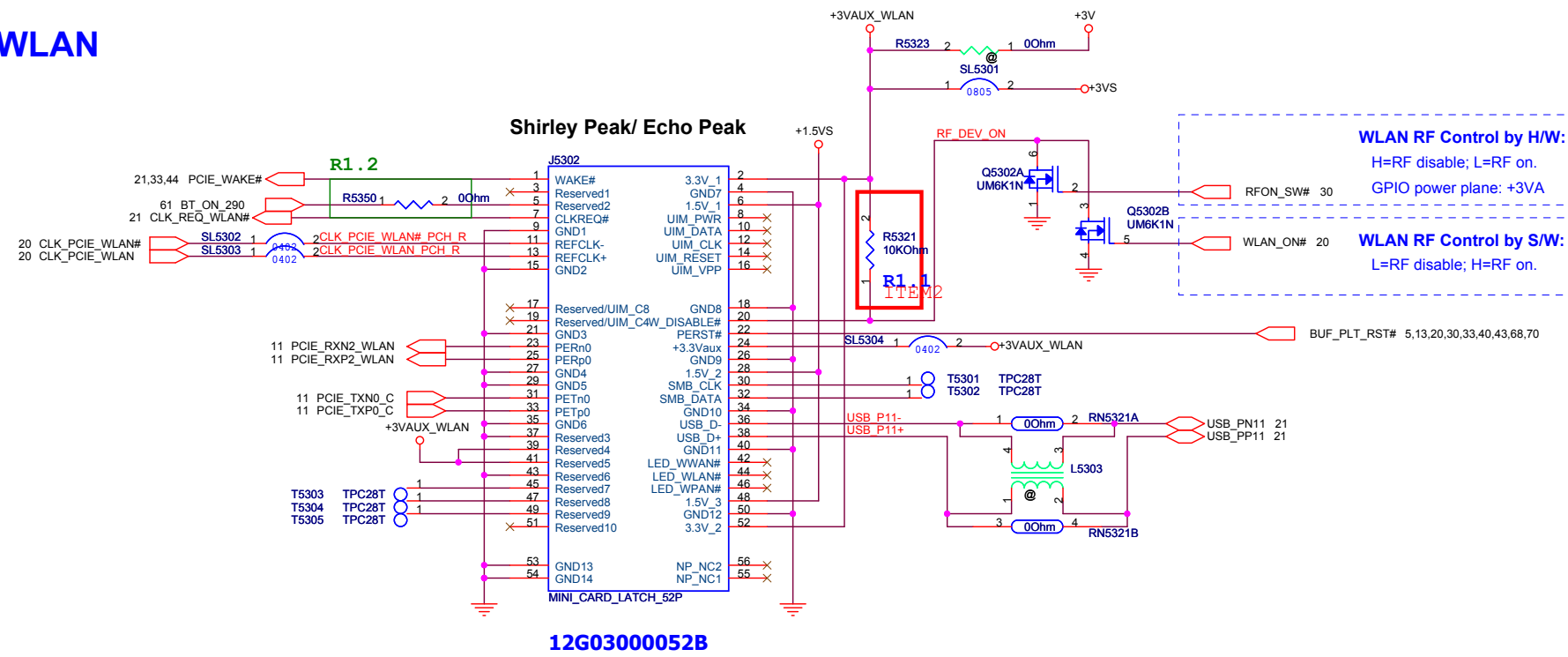
www.aitech1.ru



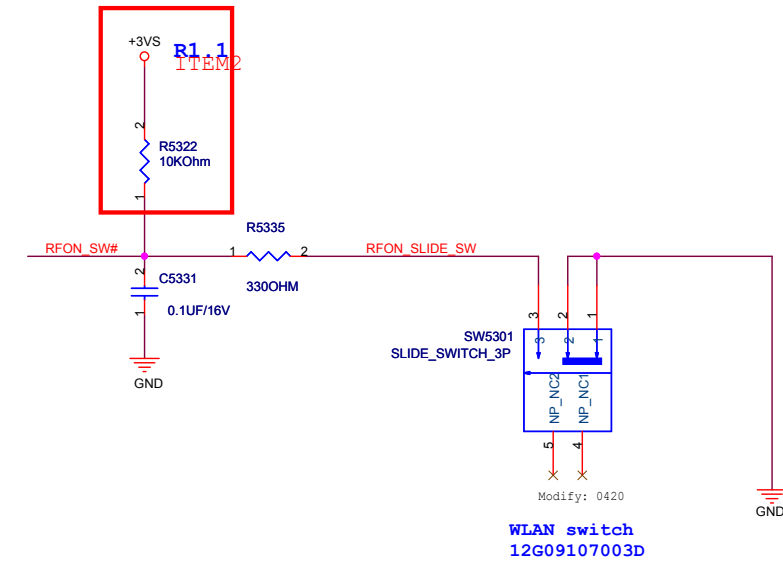
## USB3.0/USB 2.0 ESD-Protection



## WLAN

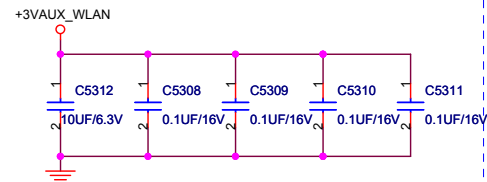


footprint使用 12G030000526  
BOM 中需帶入12G03000052B已手改



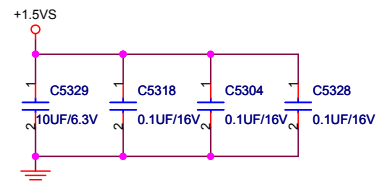
**WLAN +3VAUX bypass capactor:**

Place 0.1UF near pin 2,24,52,39 41.  
Place 10UF near +3VAUX WLAN source side.



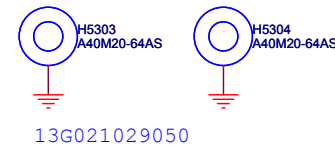
**WLAN +1.5VS bypass capactor:**

Place 0.1UF near pin 6,28,48.  
Place 10UF near +1.5VS source side.



WLAN NUT for 半卡:

```
Minicard spec R1.2:
Full size card= 2pcs.
Half size card= 2pcs.
```

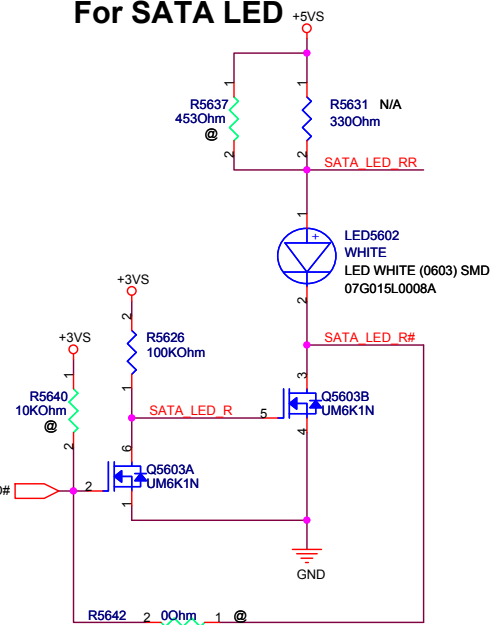


www.aitech1.ru

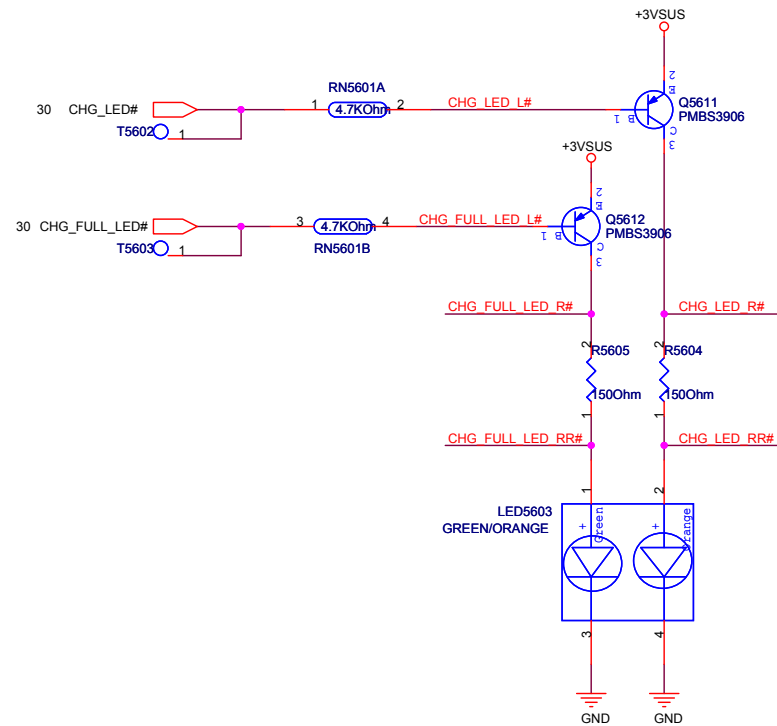


www.aitech1.ru

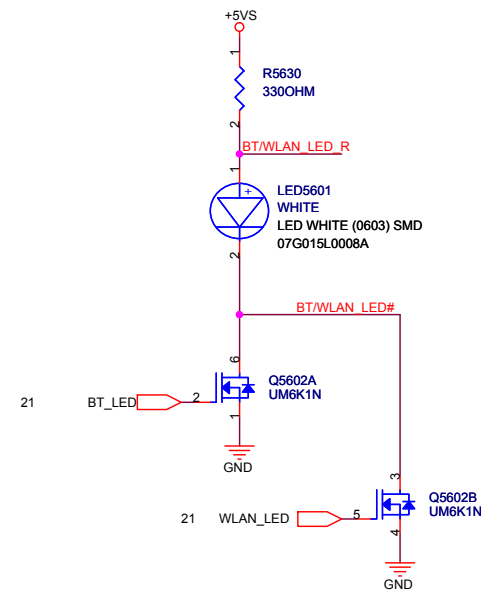
## For SATA LED



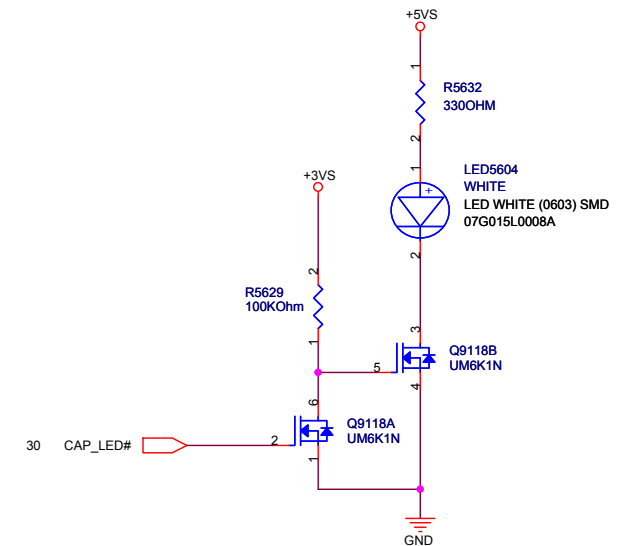
## For Battery LED



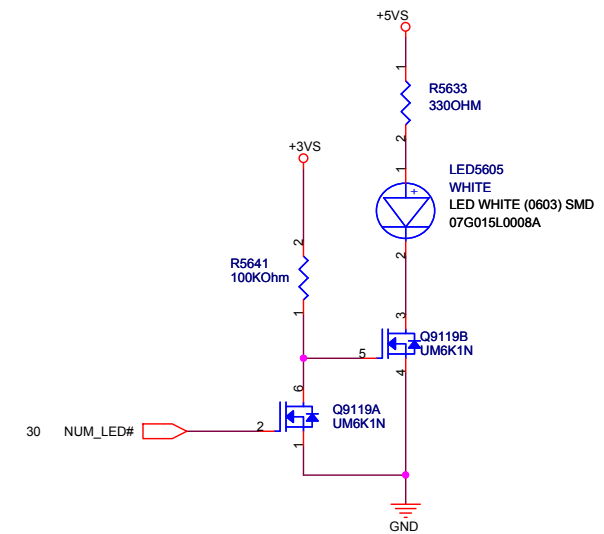
## For BT/WLAN LED



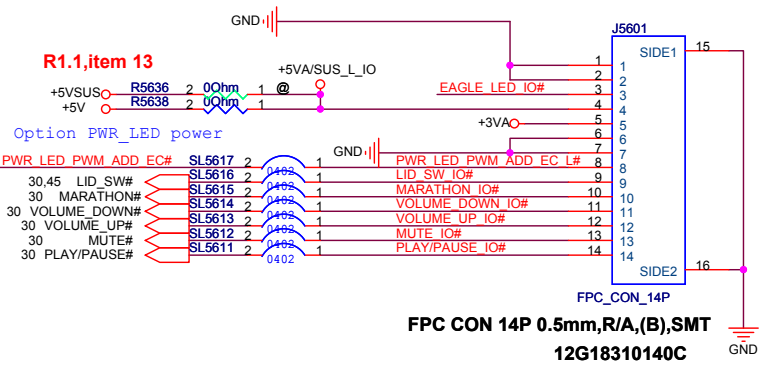
## For Caps. Lock



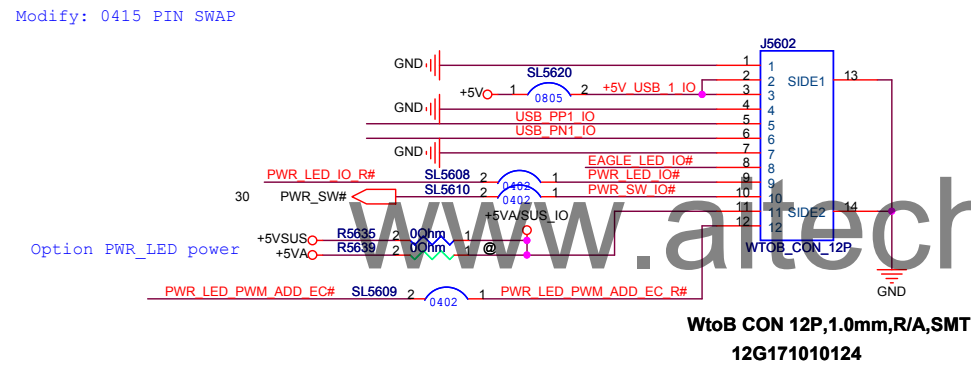
## For NUM. Lock



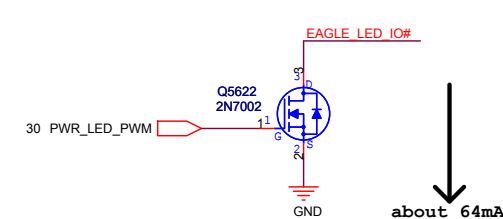
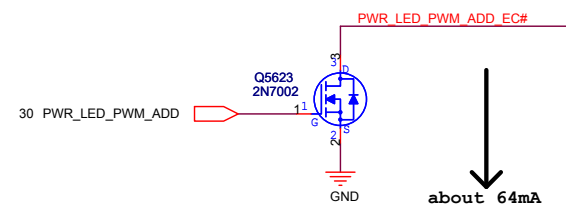
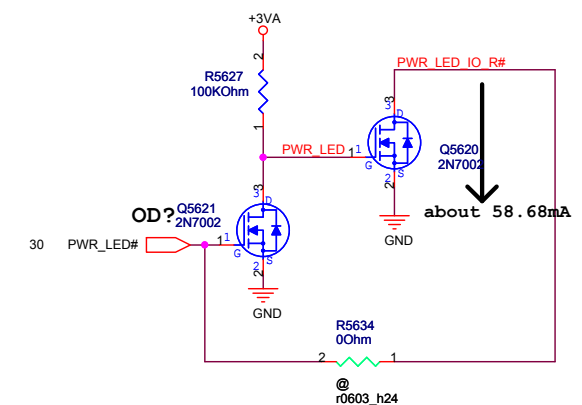
## L-SubBoard connect

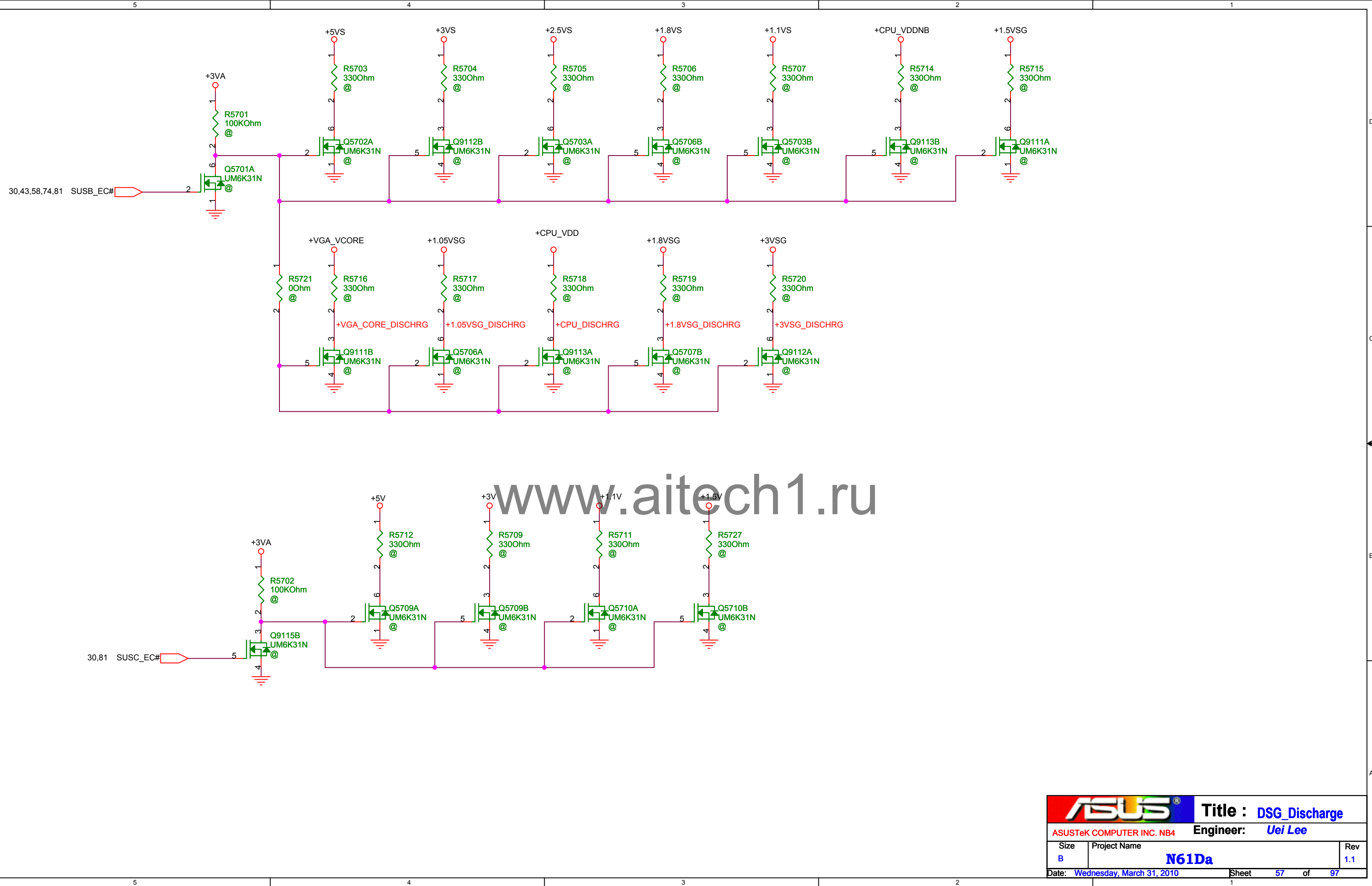


## R-SubBoard connect

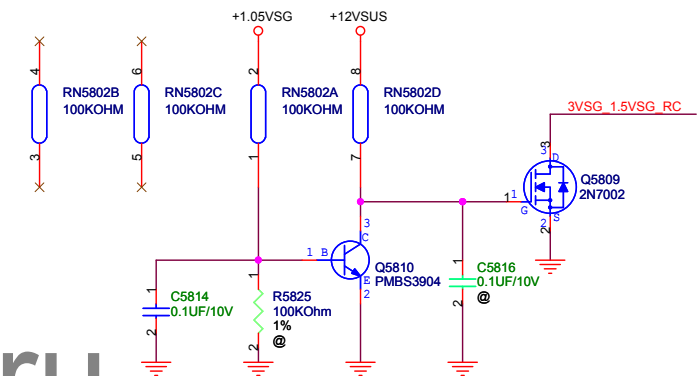
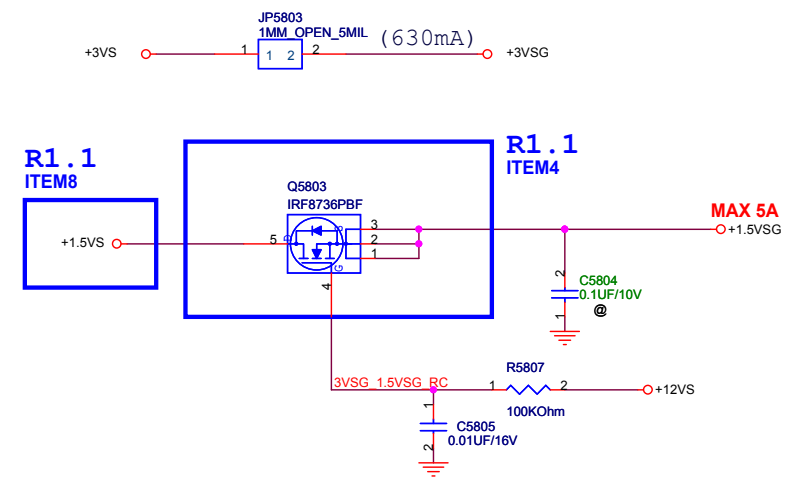
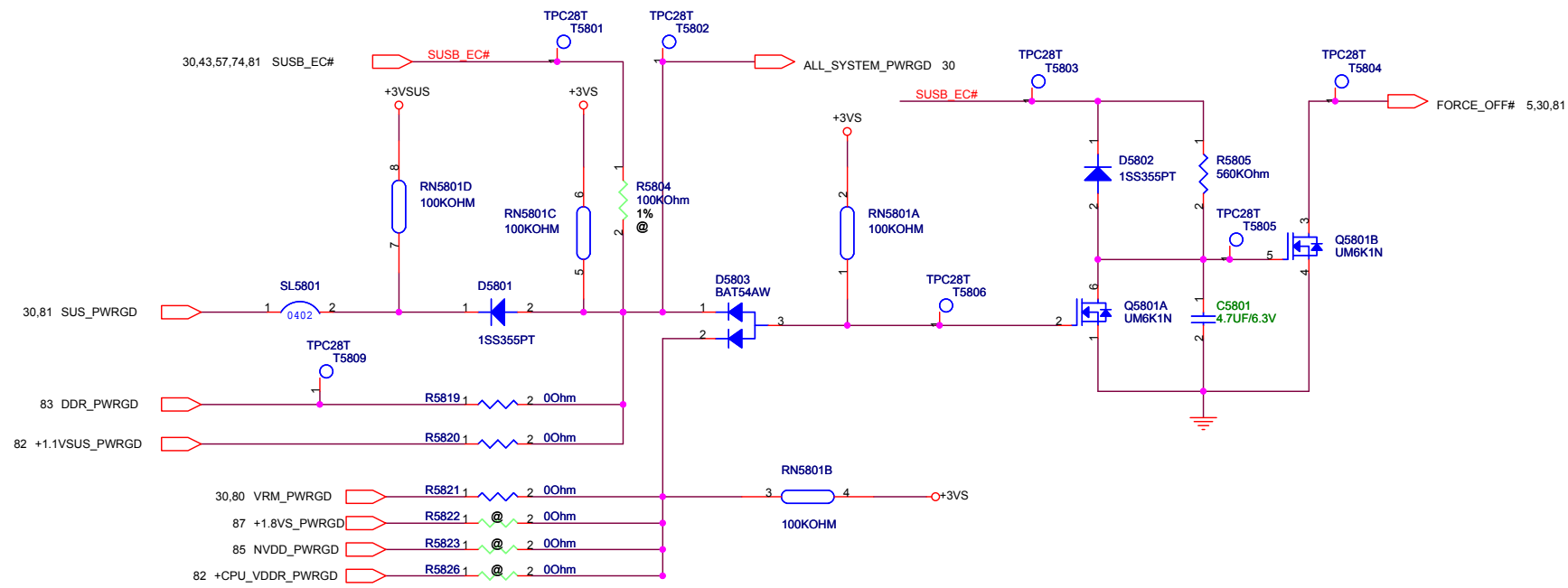


## For PWR LED






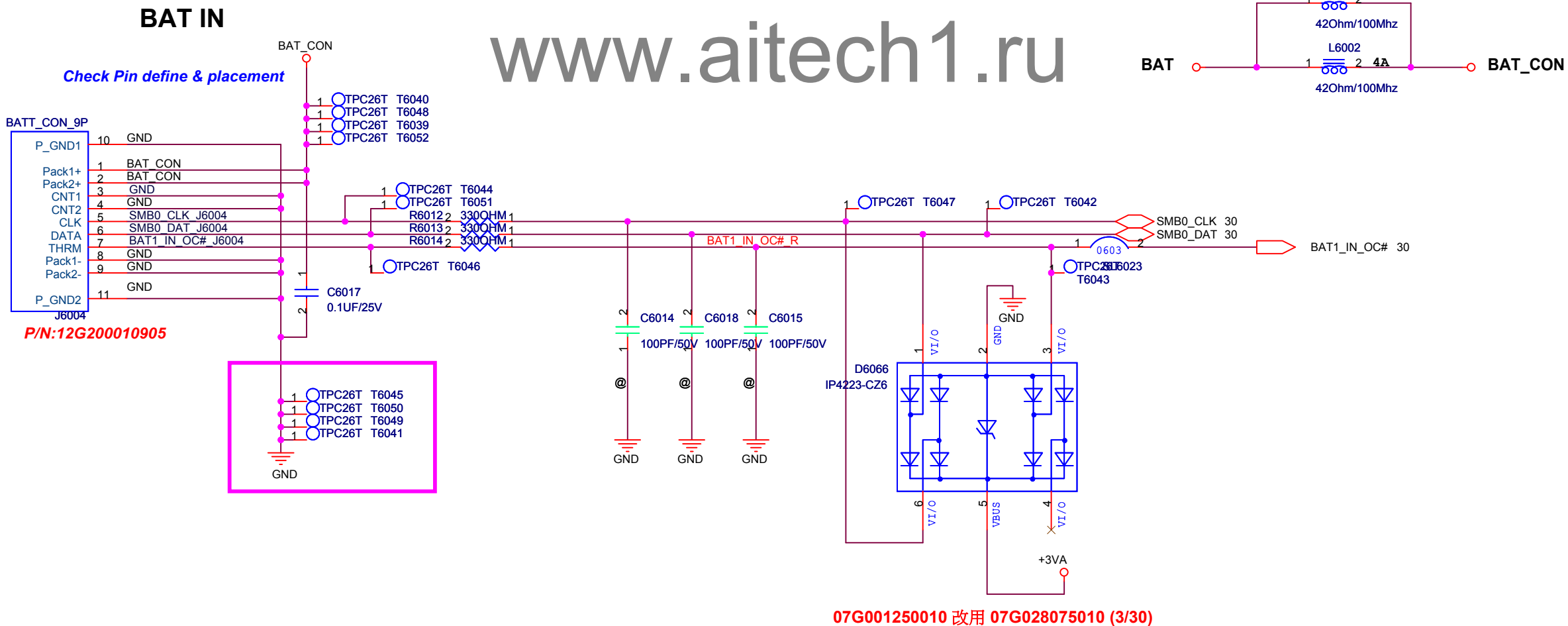
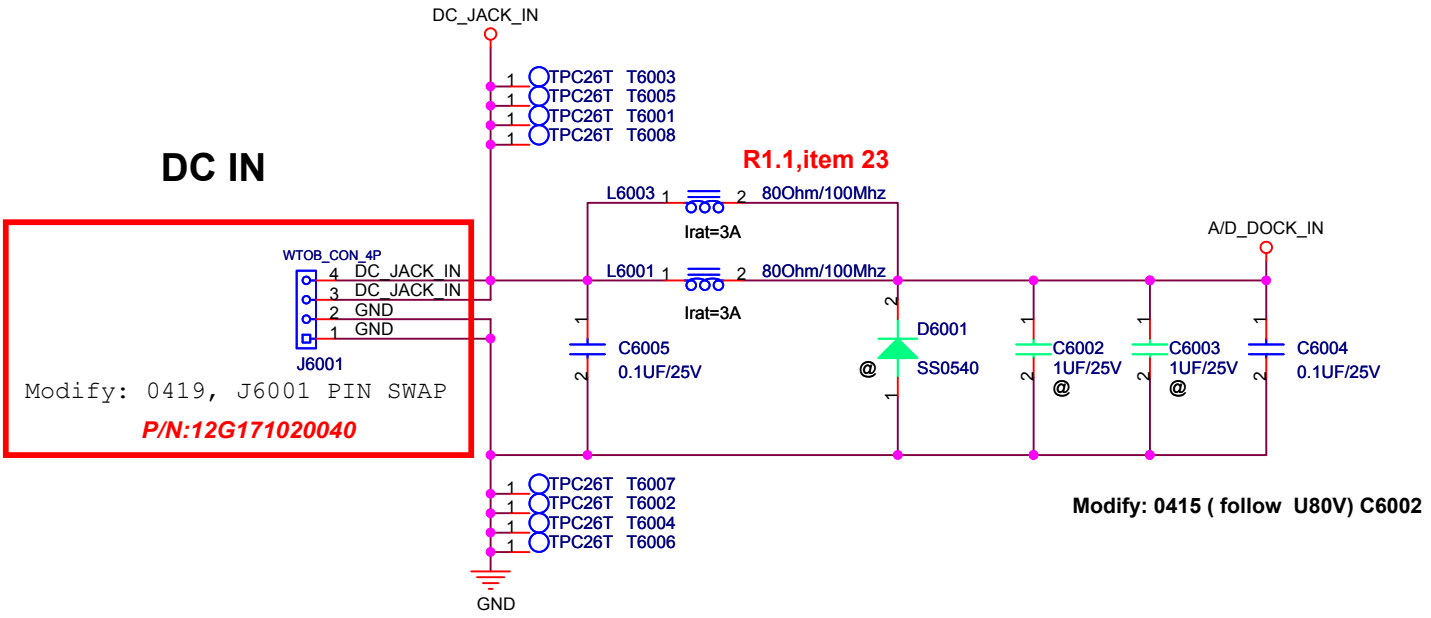
# POWER GOOD DETECTOR

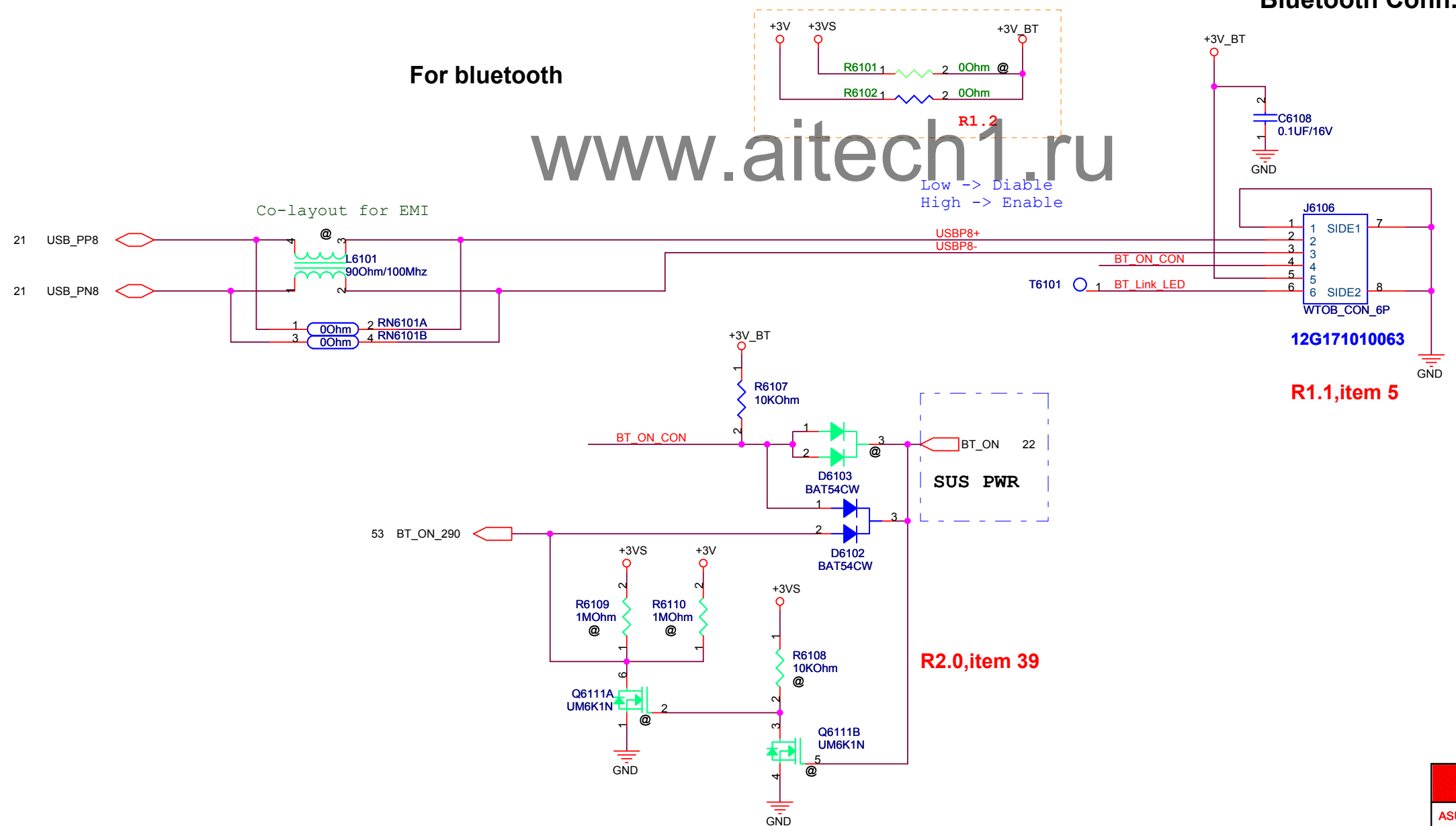


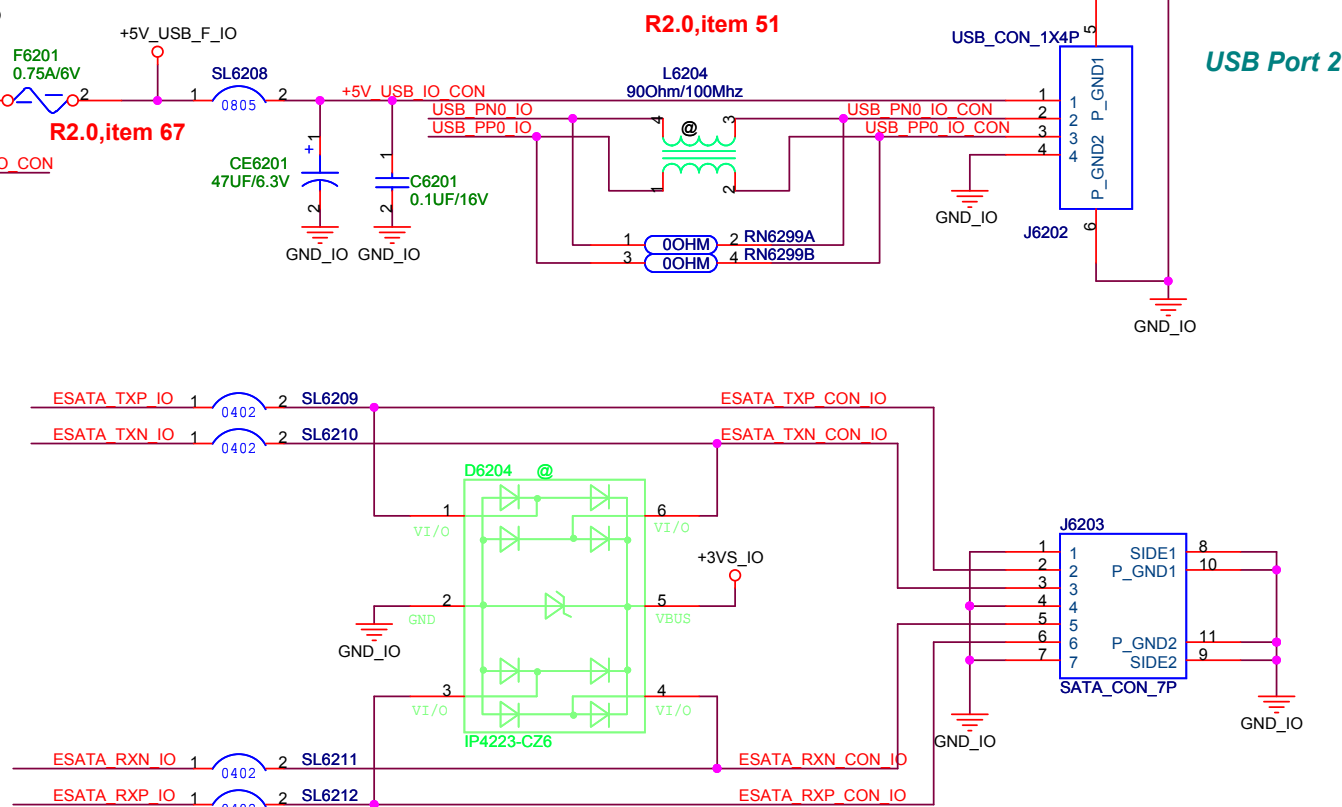
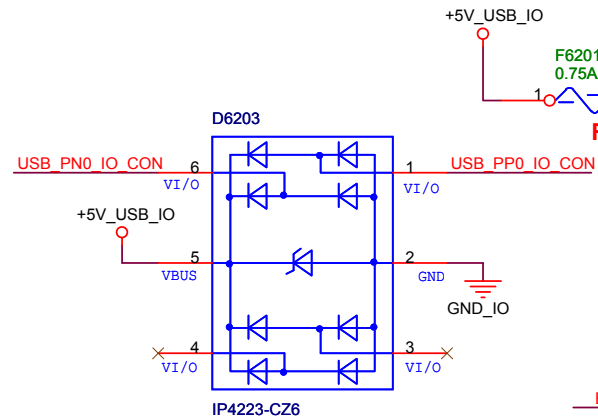
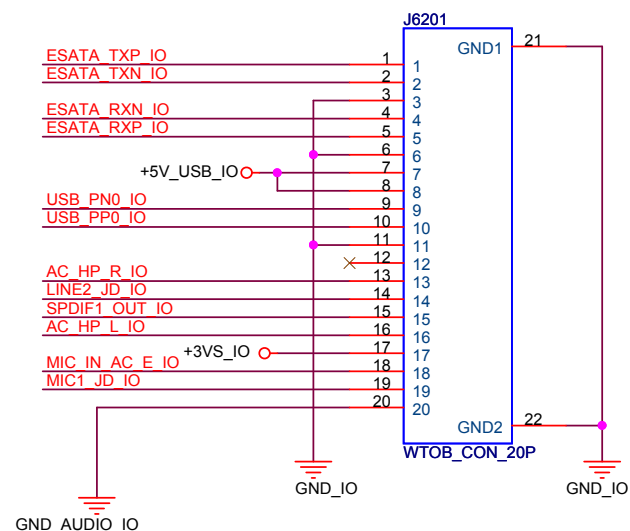
www.aitech1.ru

www.aitech1.ru

		Title : DJ_****	
ASUSTeK COMPUTER INC. NB4		Engineer: Uei Lee	
Size A	Project Name N61Da		Rev 1.1
Date: Tuesday, March 30, 2010		Sheet 59 of 97	

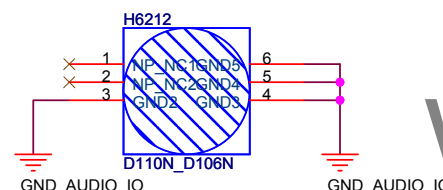
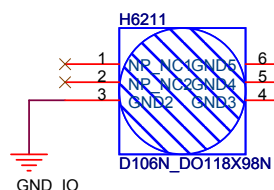






S04169

S04168

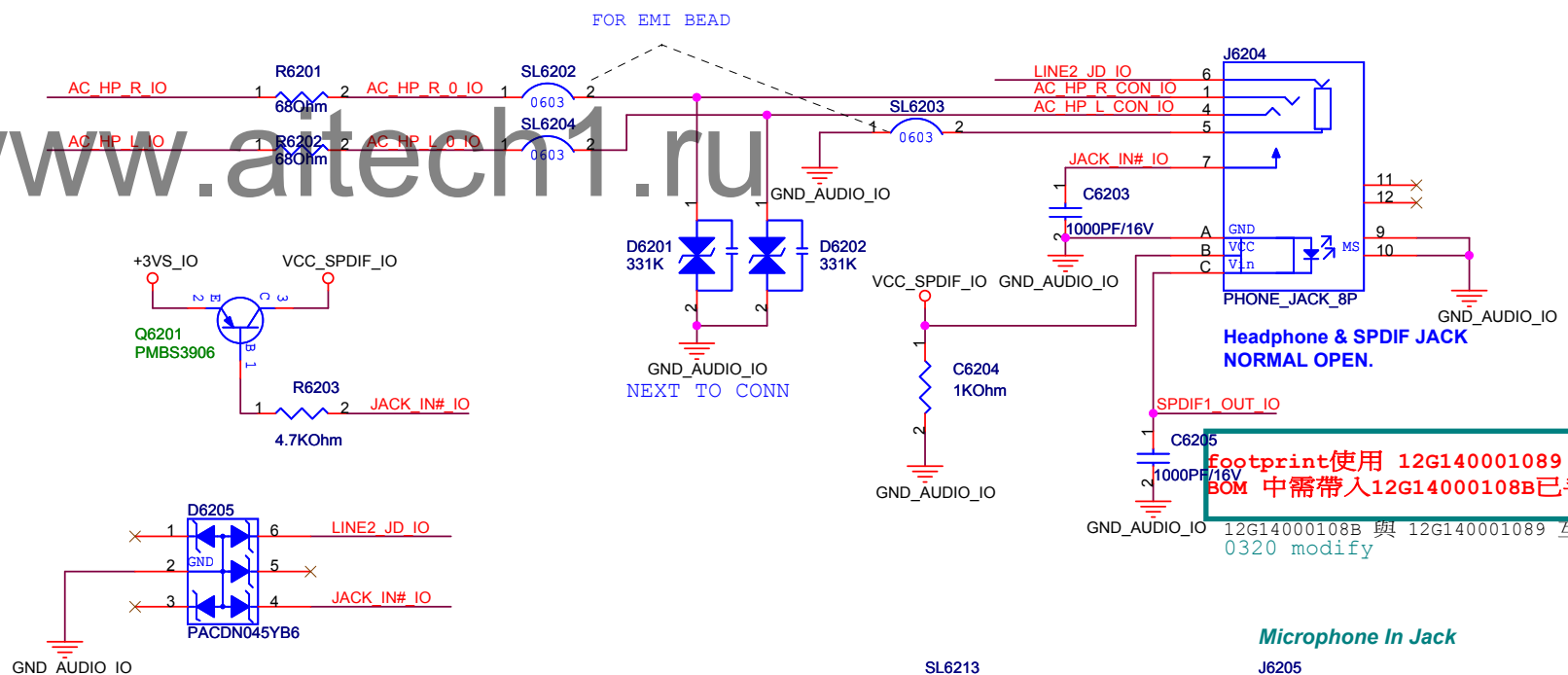


temp\_3815\_gw44

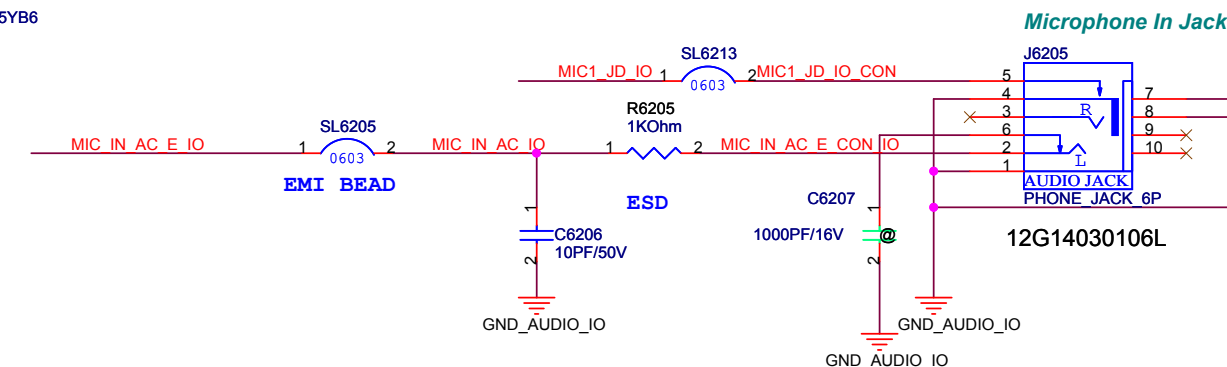
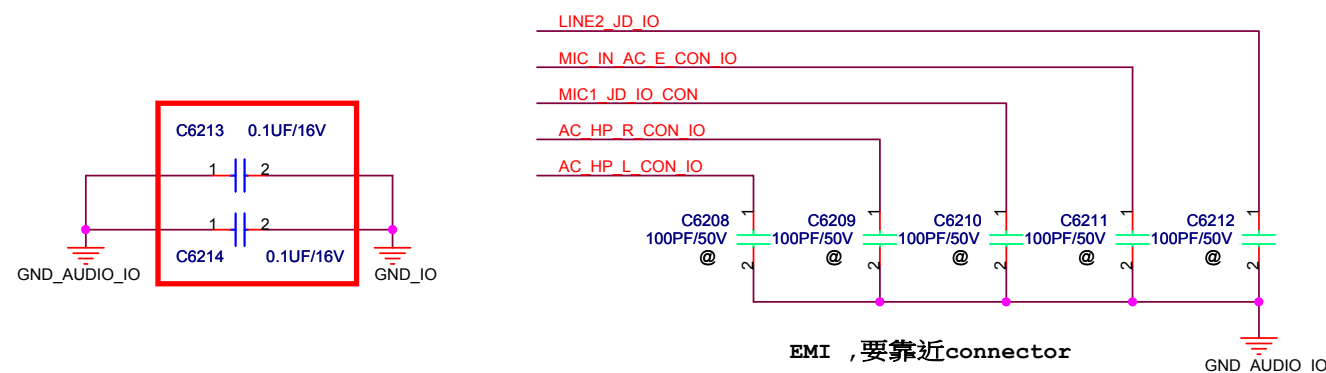


0414 modify

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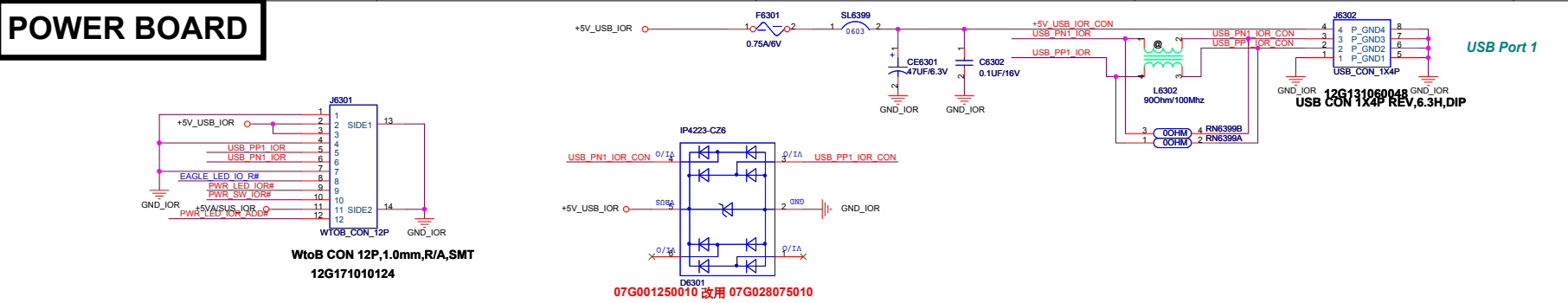


footprint使用 12G140001089  
BOM 中需帶入12G14000108B已手改  
12G14000108B 與 12G140001089 互為替代  
0320 modify

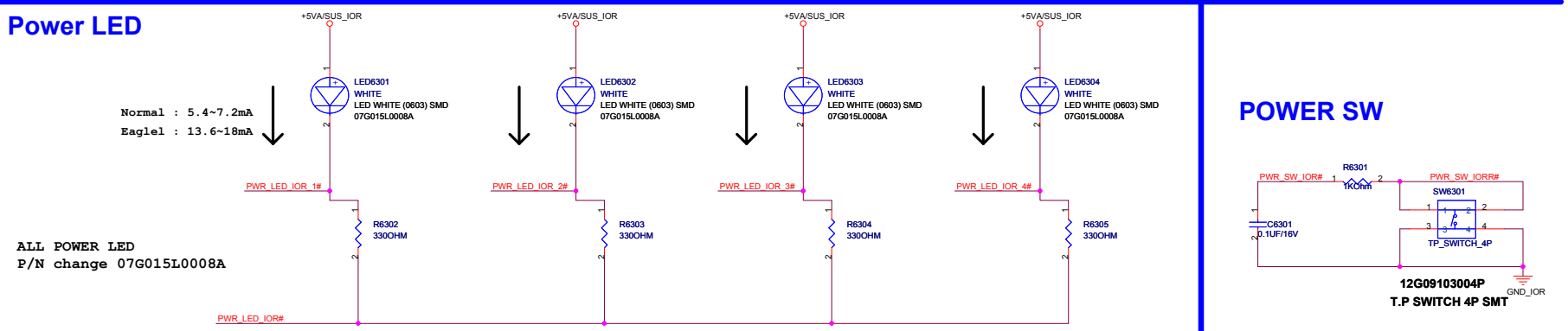




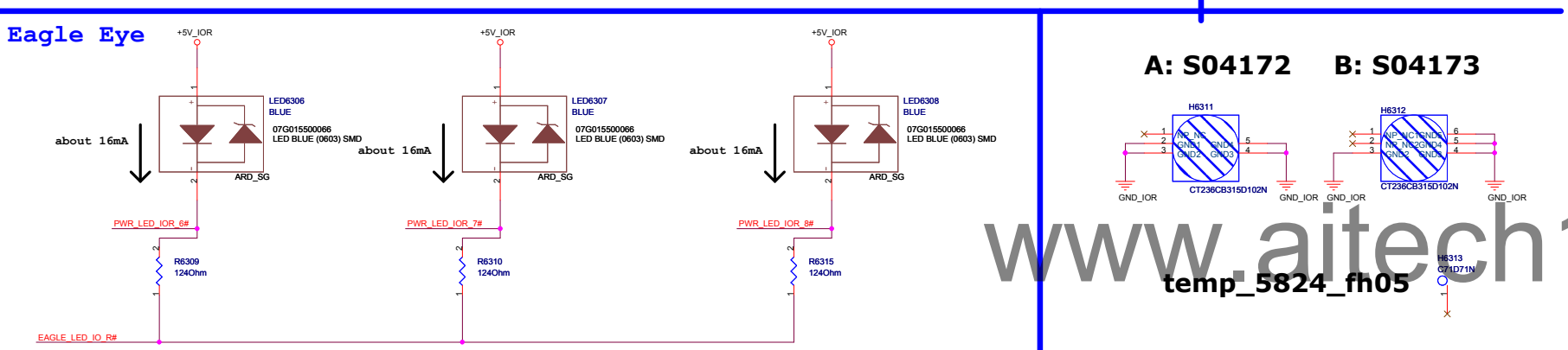
POWER BOARD



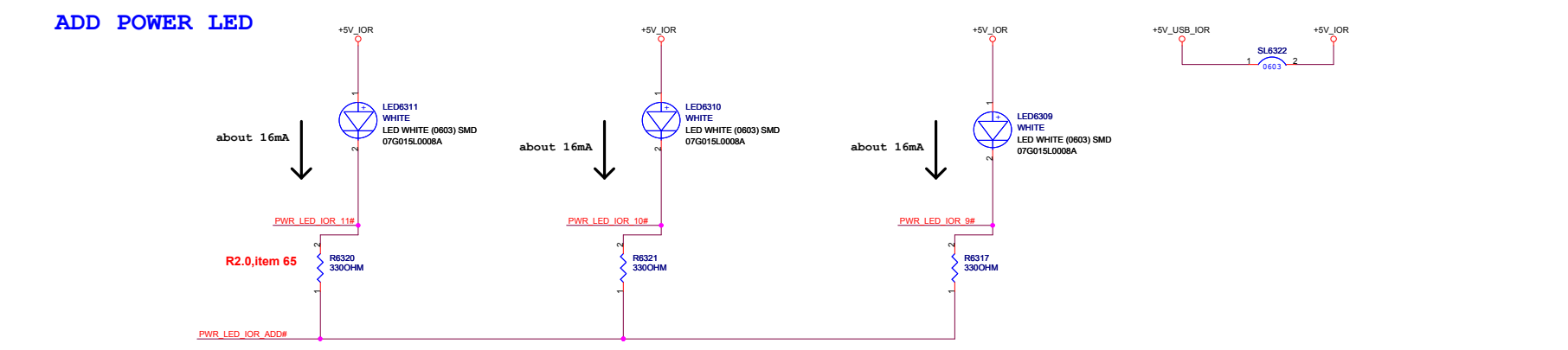
Power LED



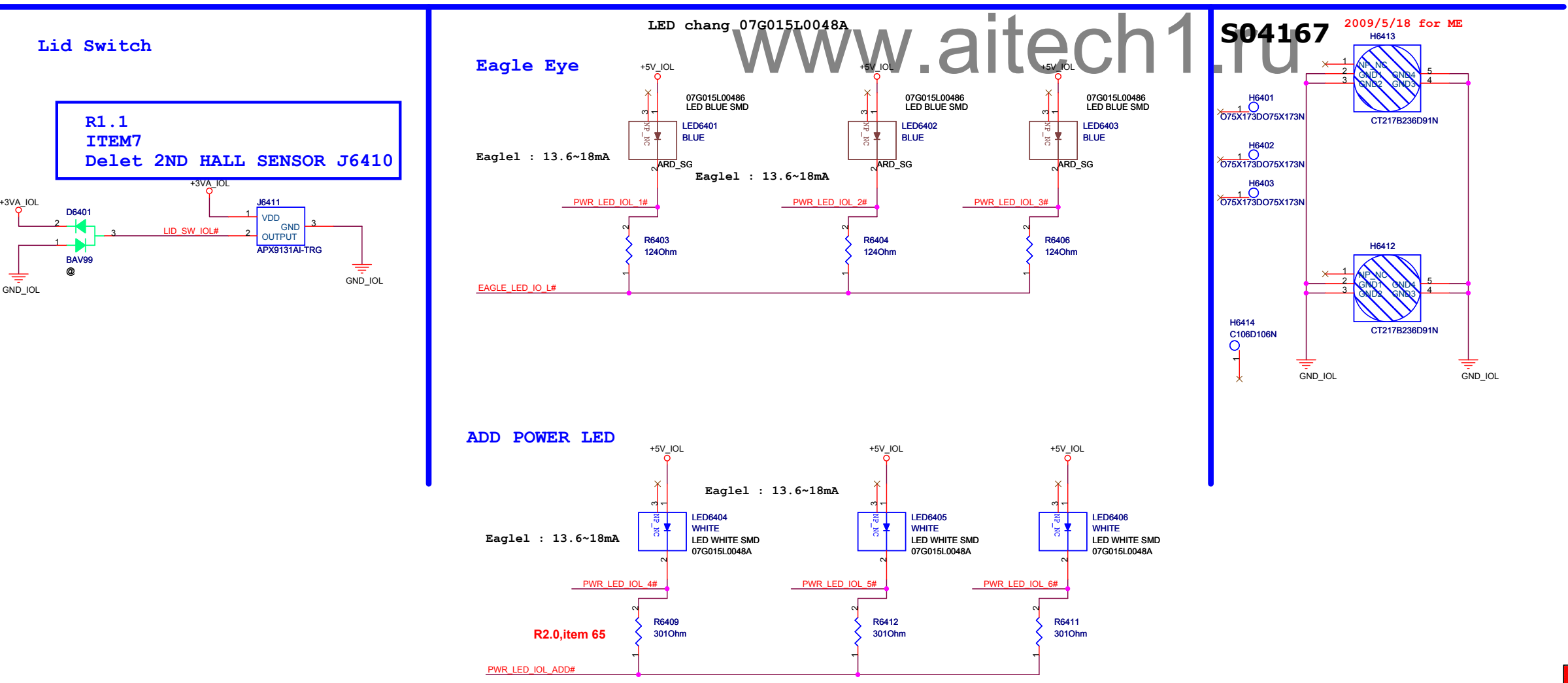
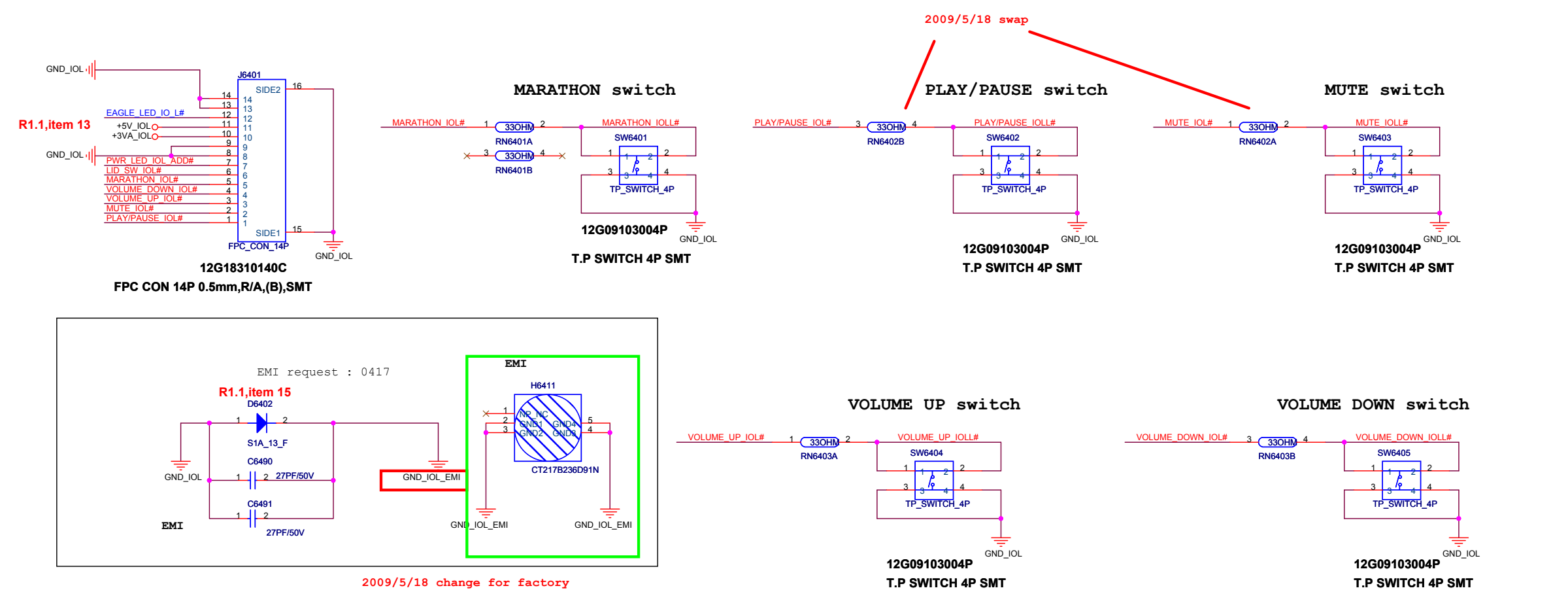
Eagle Eye



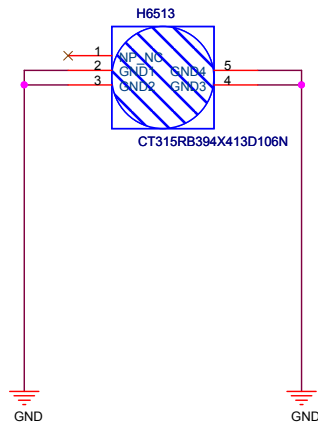
ADD POWER LED



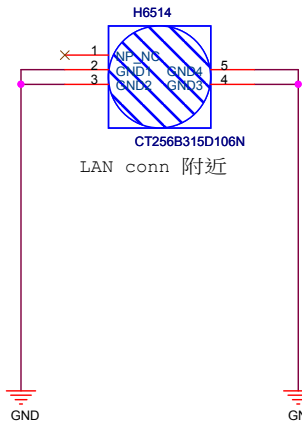
FUNCTION BOARD



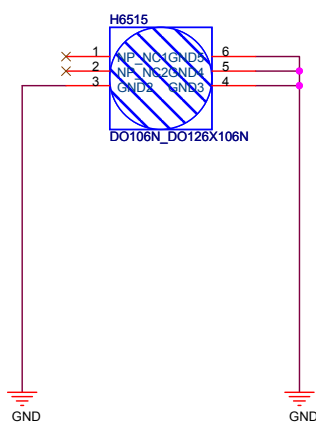
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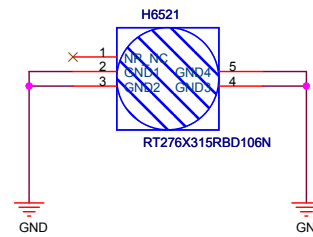
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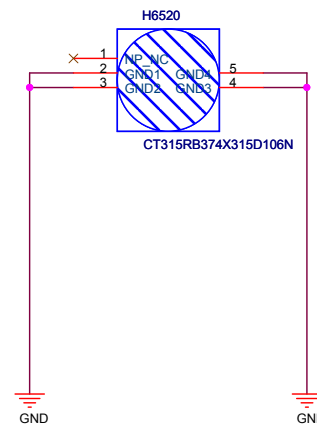
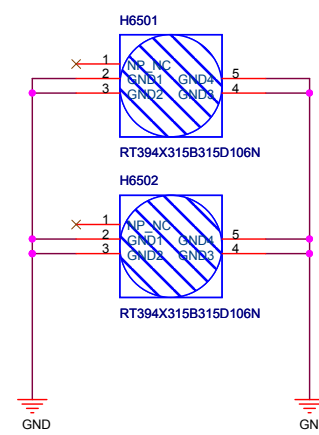
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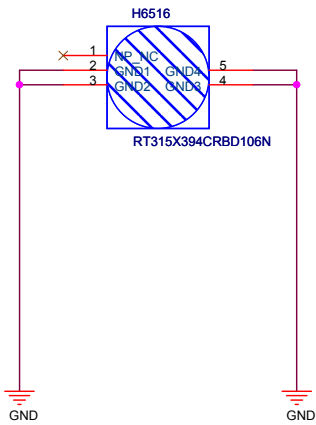
## L



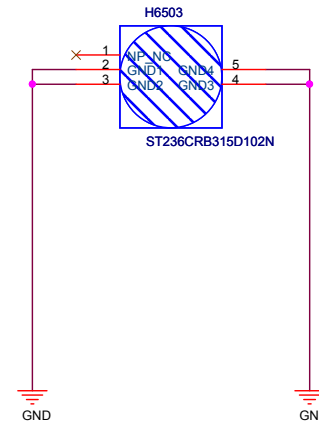
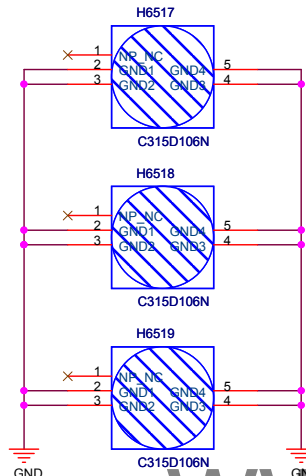
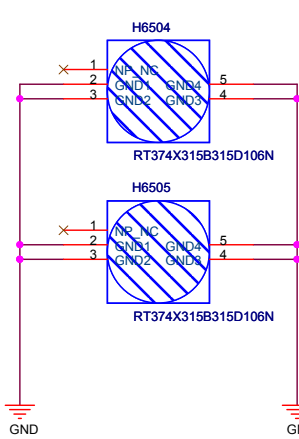
## B



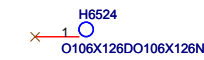
## N: S04159



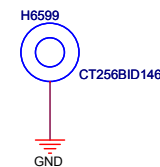
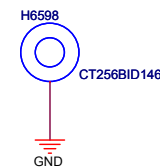
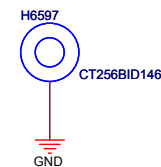
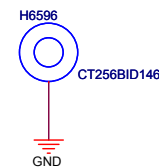
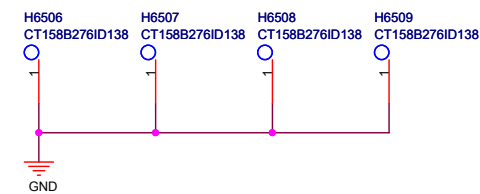
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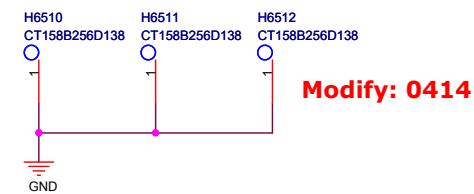
## HOLD



## CPU ( F : S04153 )

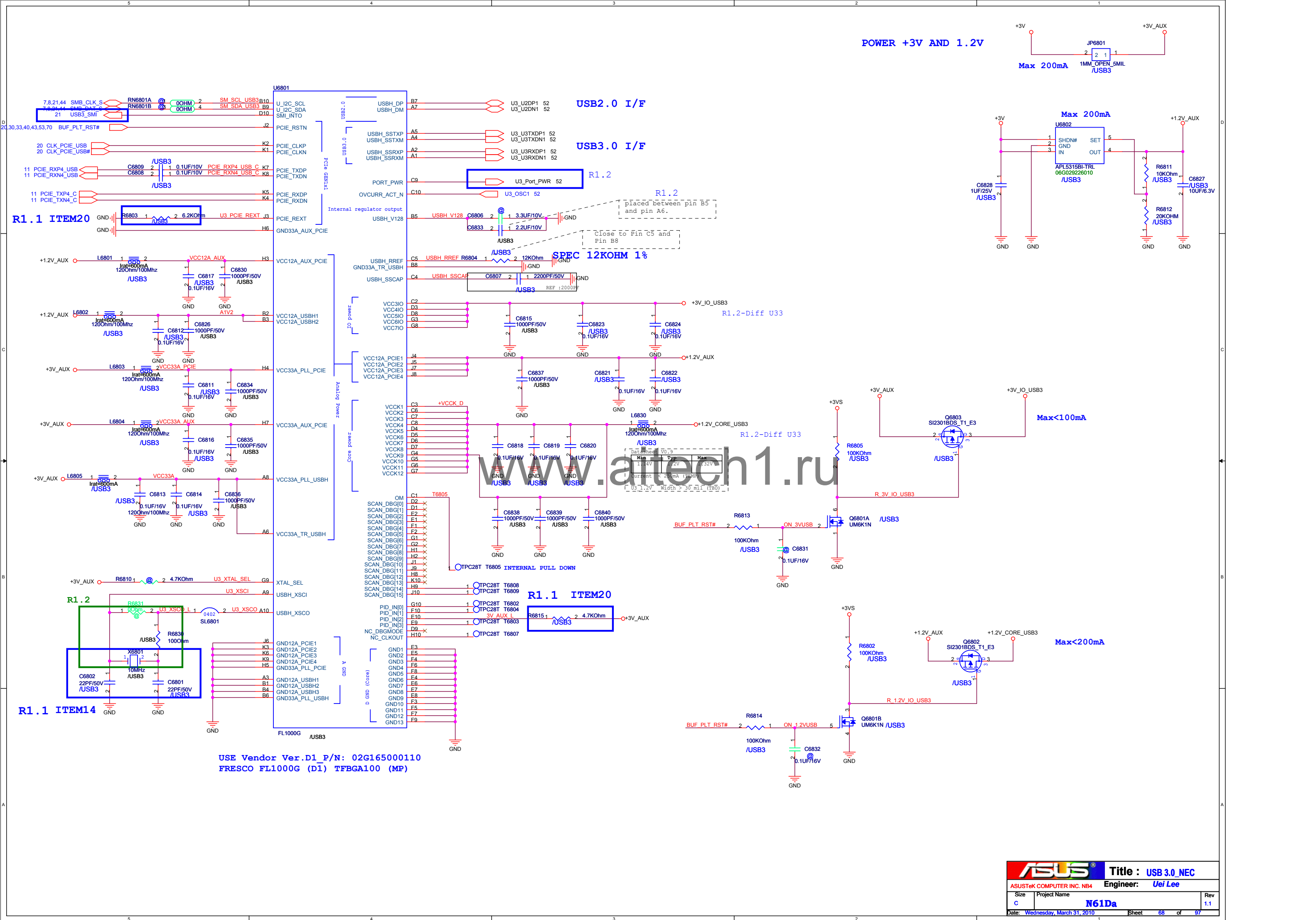


## GPU ( G : S04170 )

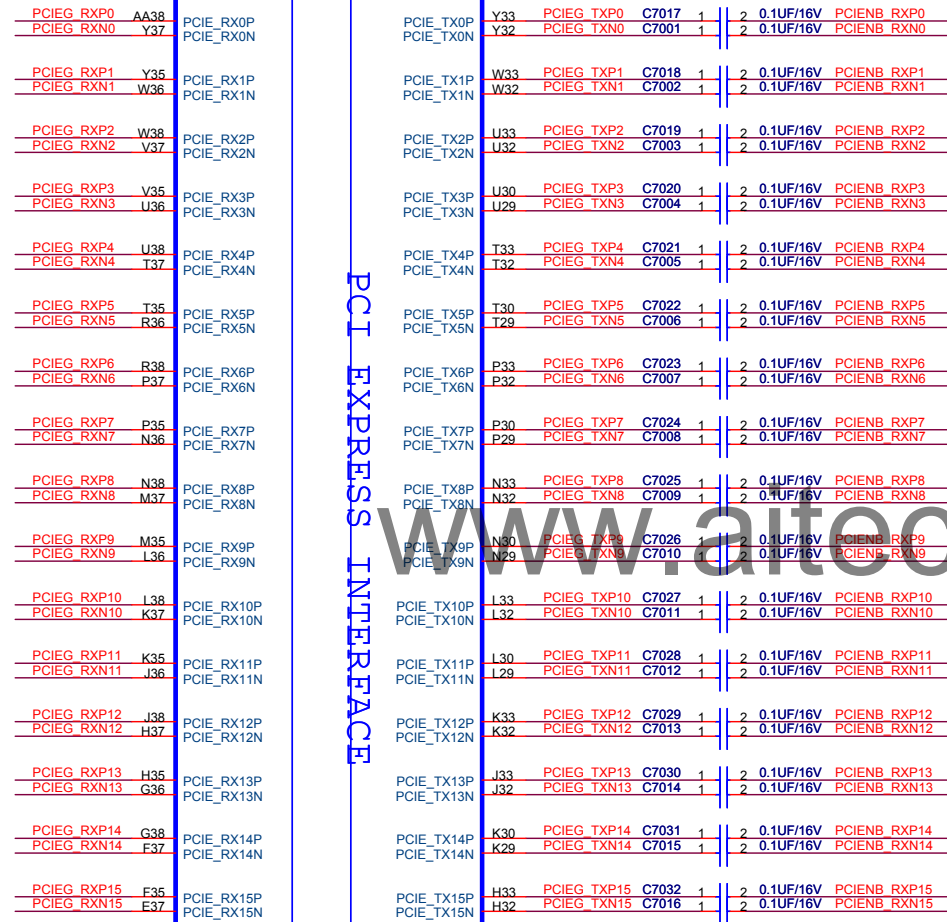
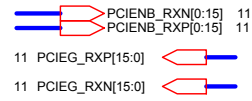


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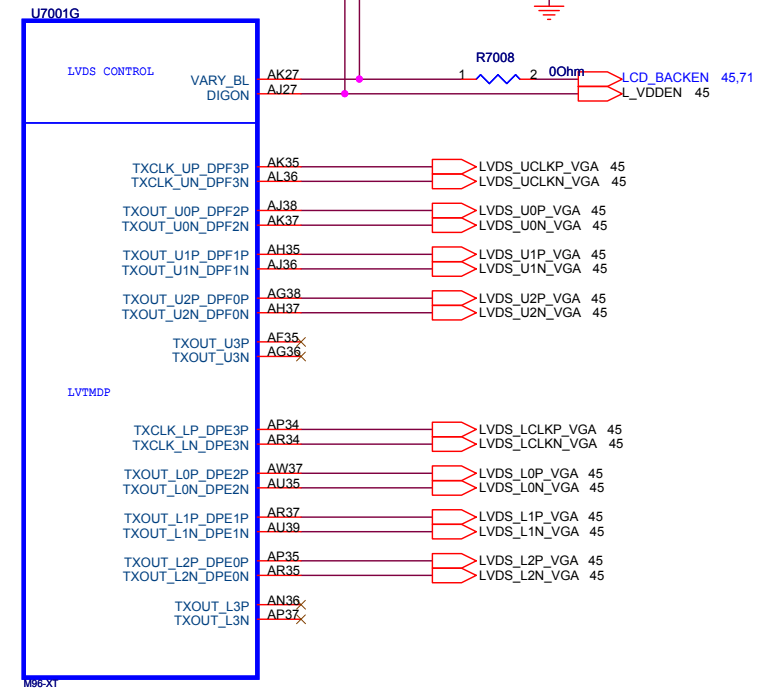
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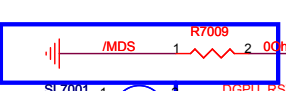


PCI EXPRESS INTERFACE

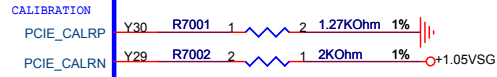


20 CLK\_PCIE\_PEG  
20 CLK\_PCIE\_PEG#

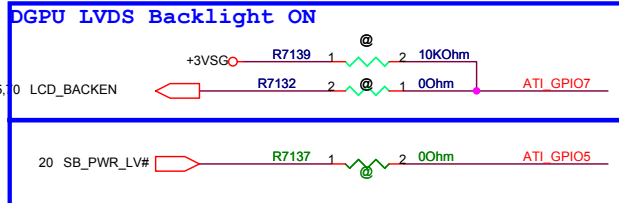
R1.1  
M96



BAILL AH16  
M96-M2 NC  
MADISON-M2 GND

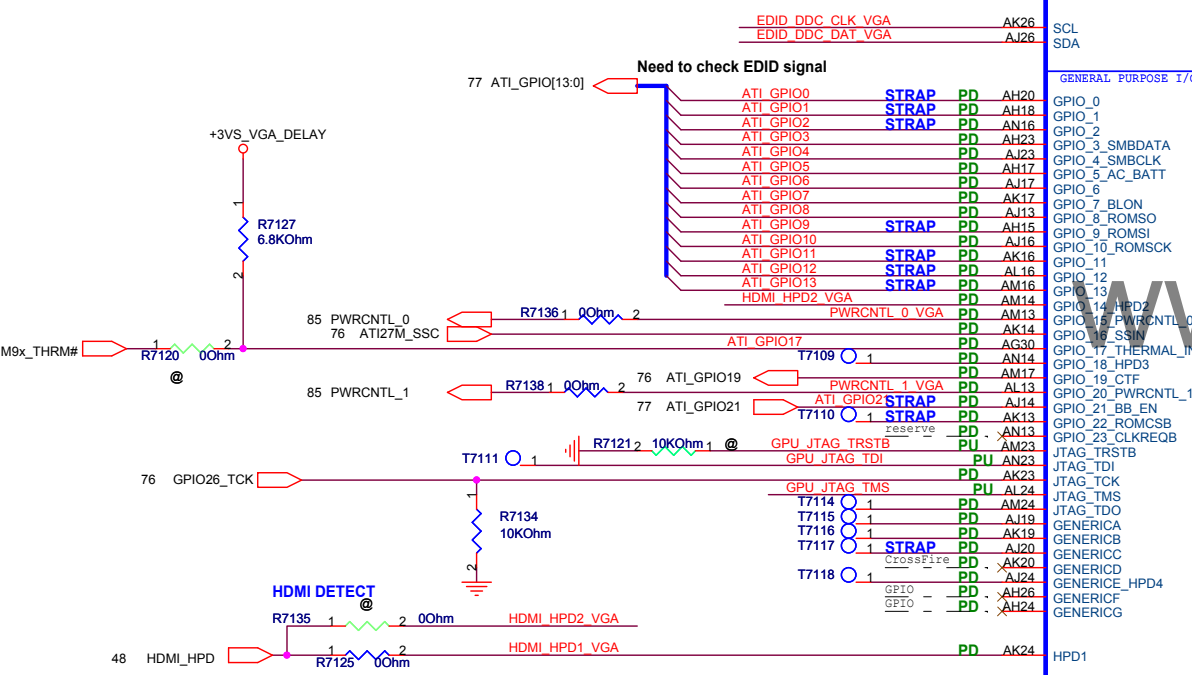
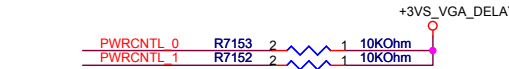






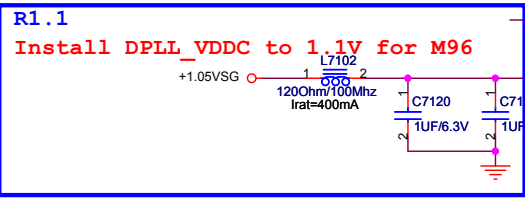
SB\_PWR\_LV 在G73是接到GPU GPIO5 AC\_BAT PIN 但N71JA 这支GPIO 不接,AC/DC MODE 功能仍正常

PWRCNTL_1	PWRCNTL_0	+NVDD
1	1	1.1V
1	0	1.05V
0	1	0.95V
0	0	0.9V



For M76M/M86/M96 VREFG voltage is 0.6V(VR59 take away,VR287=249ohm)

Install DPLL\_PVDD to +1.8V for M96

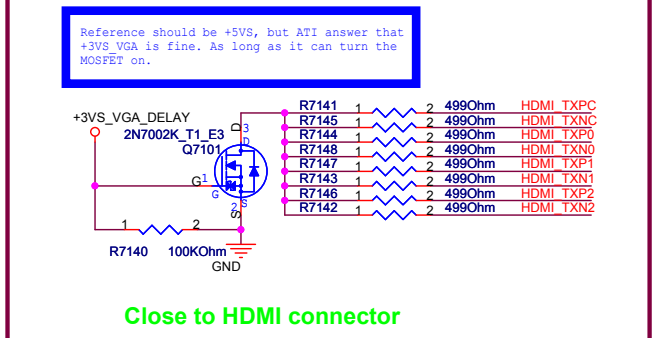
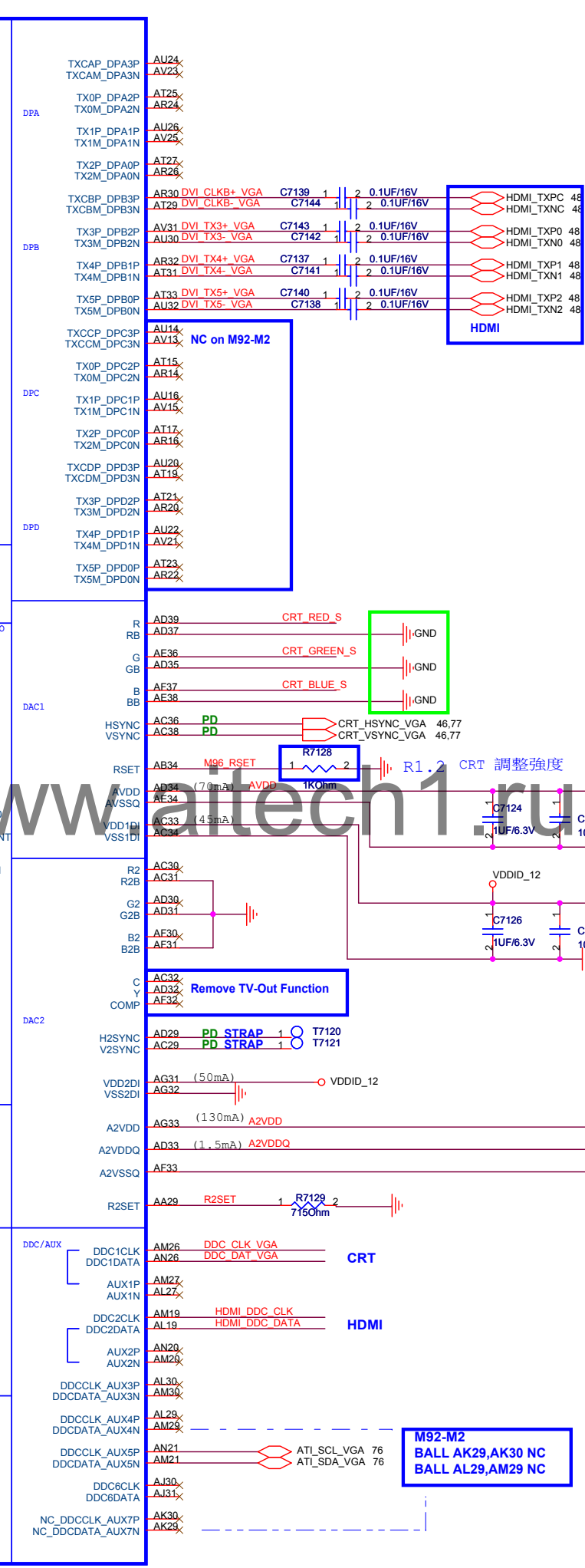


Install DPLL\_PVDD to +1.8V for M96

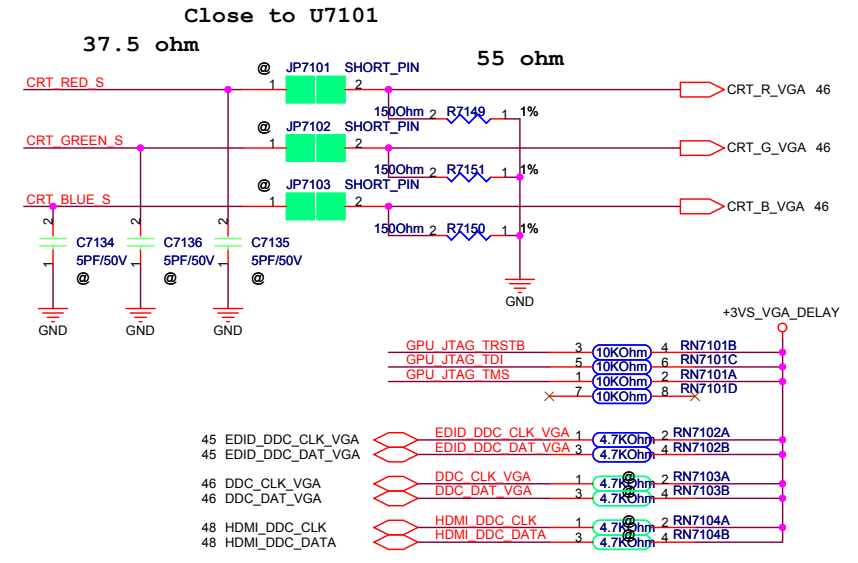
Install DPLL\_PVDD to +1.8V for M96

Install DPLL\_PVDD to +1.8V for M96

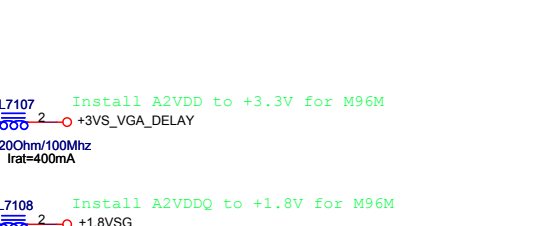
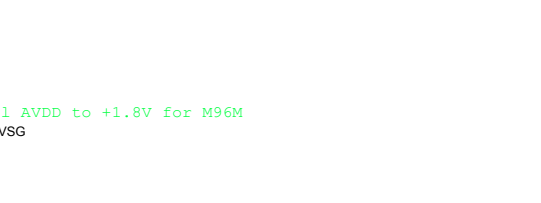
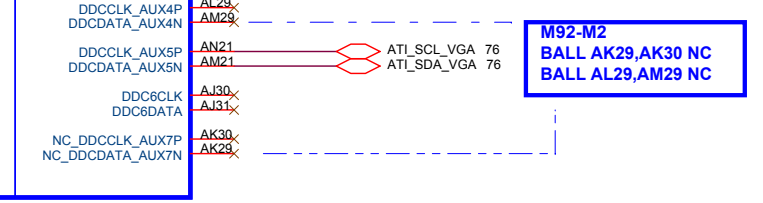
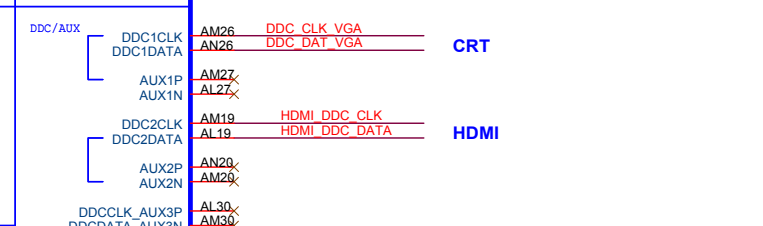
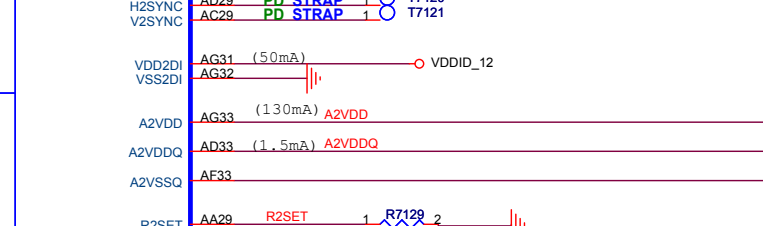
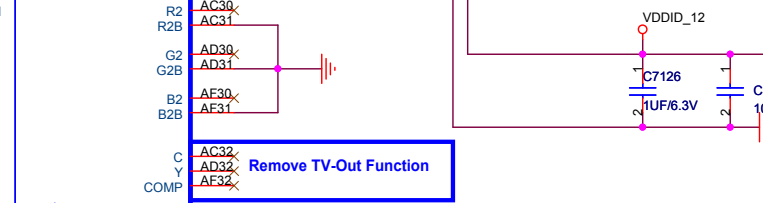
Install DPLL\_PVDD to +1.8V for M96

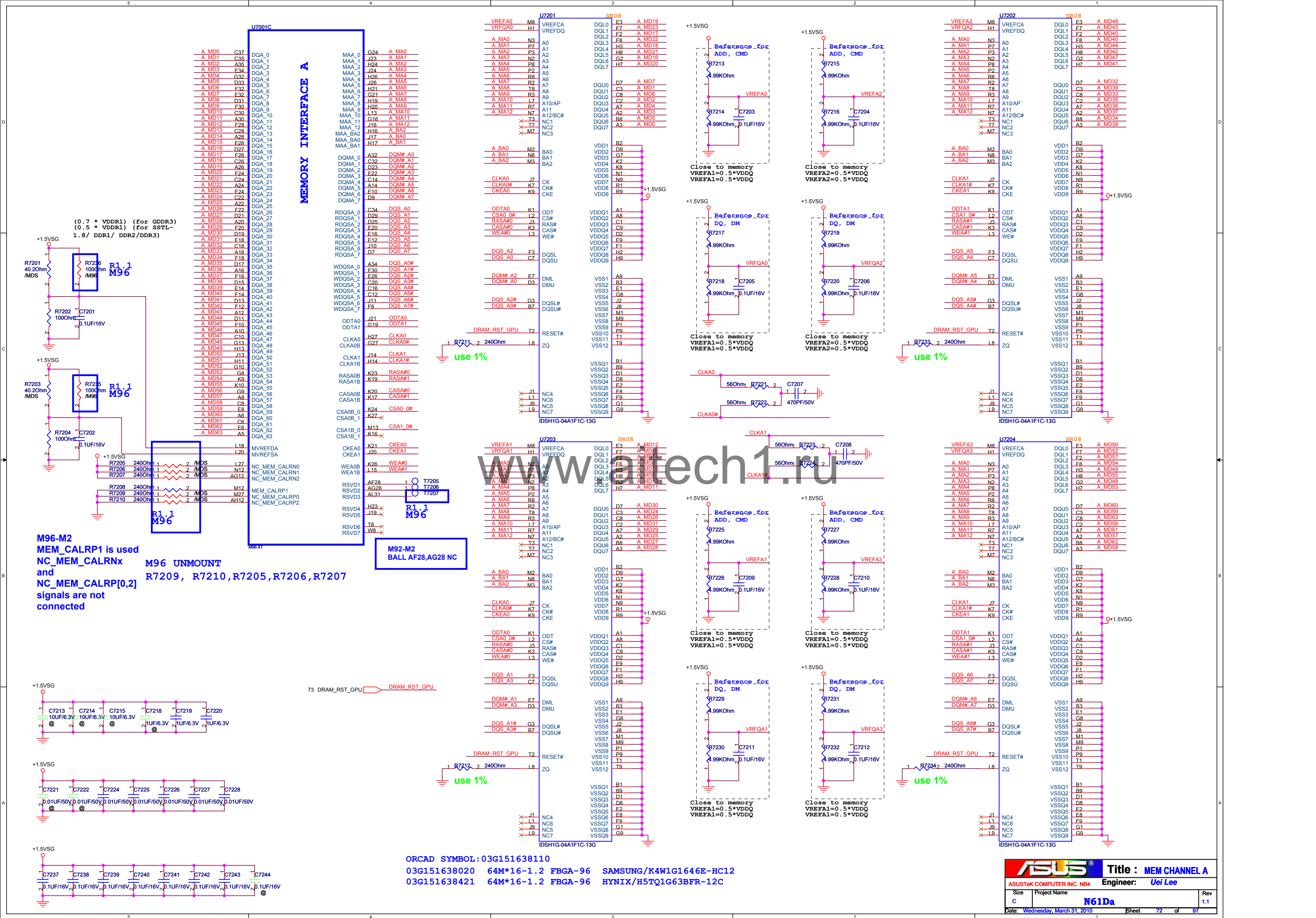


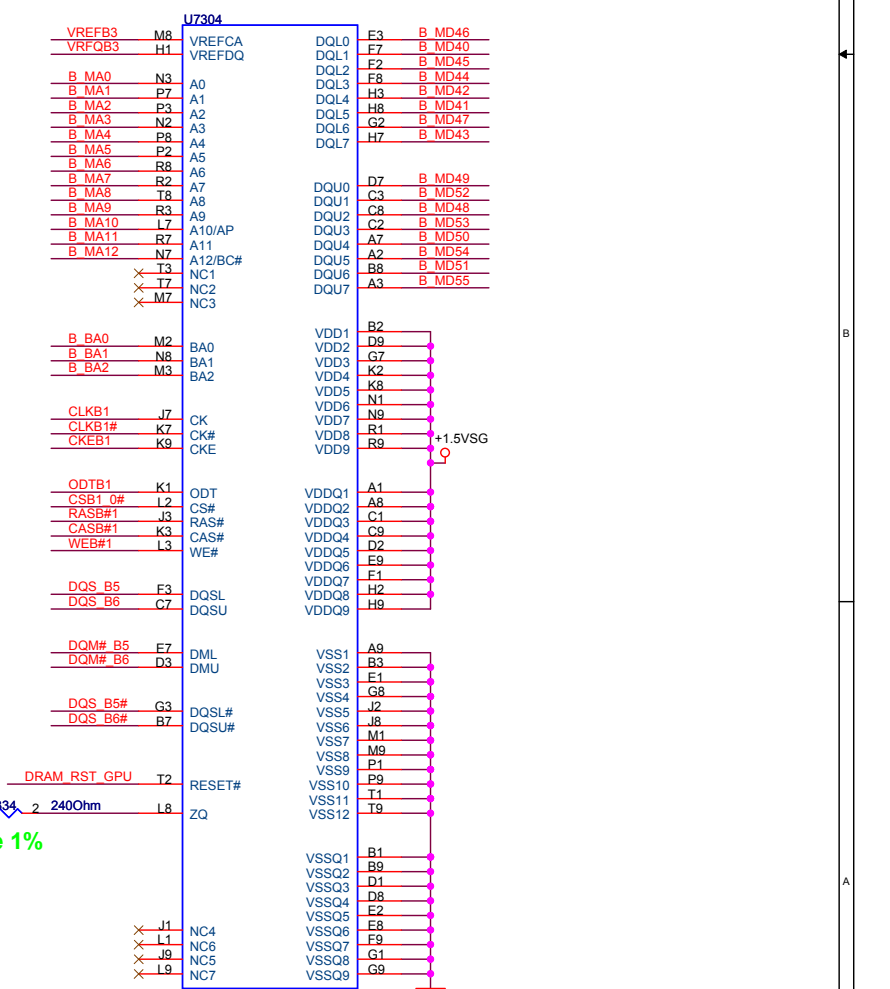
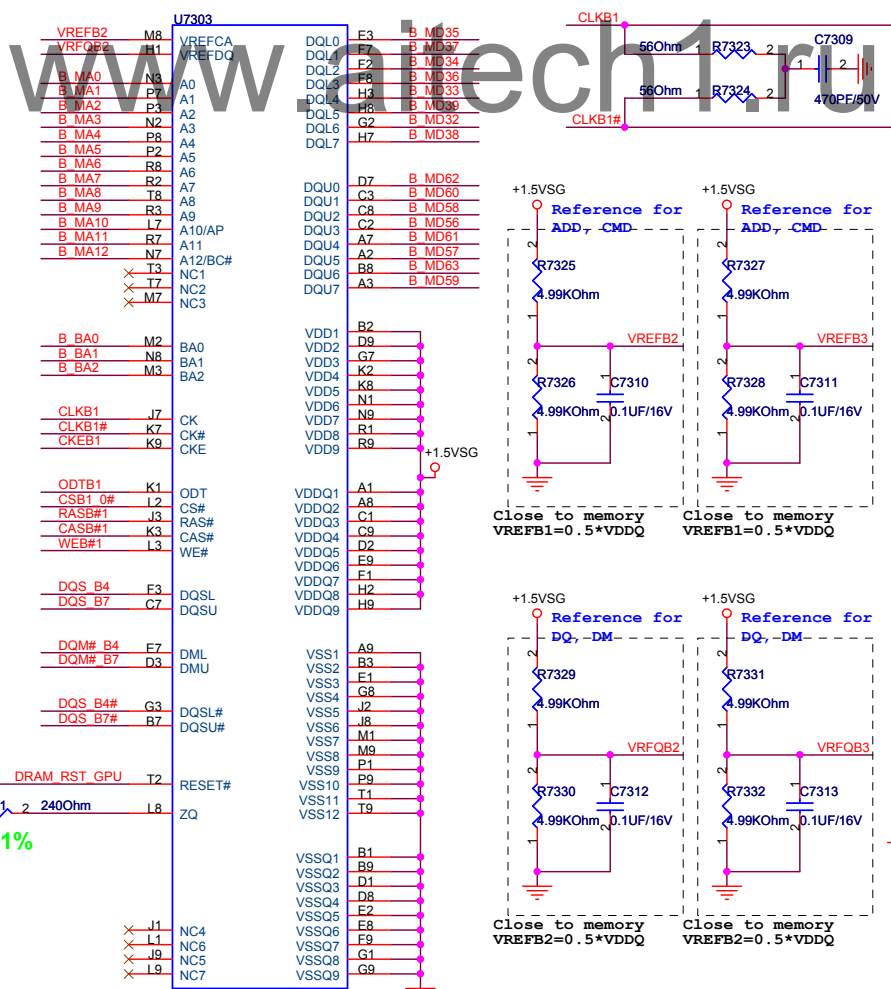
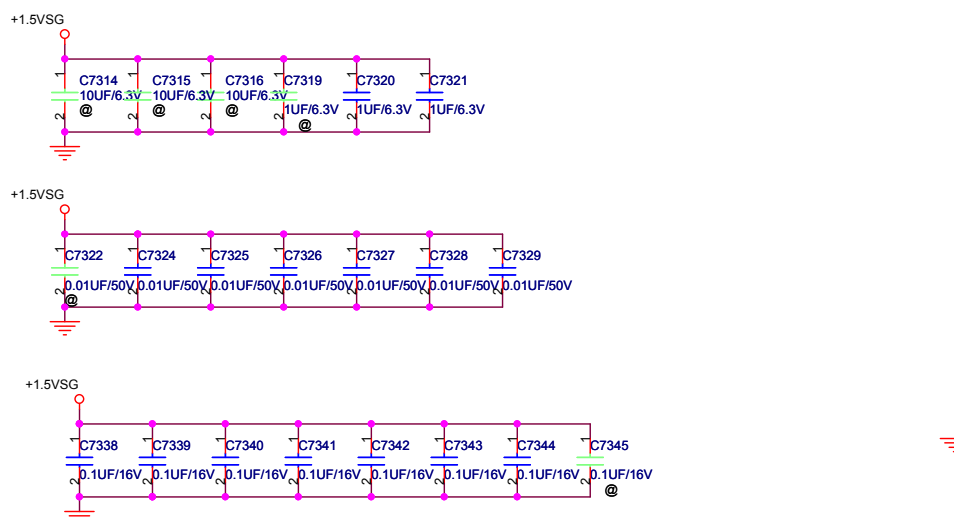
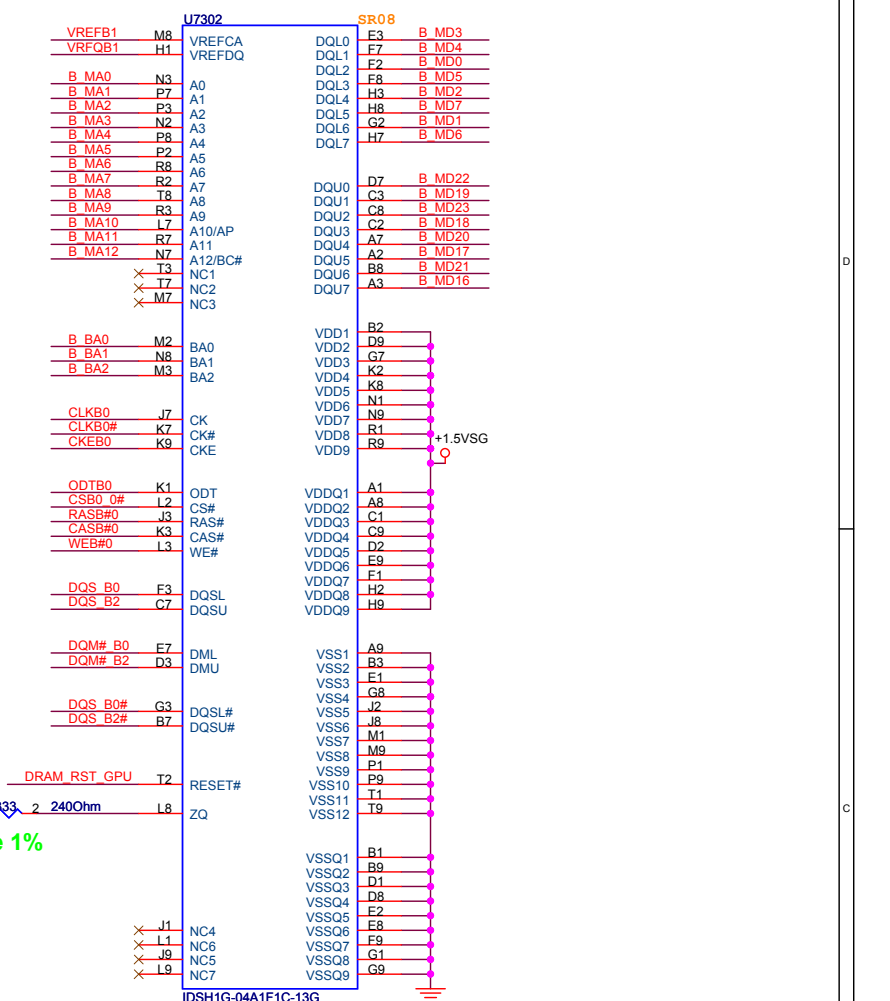
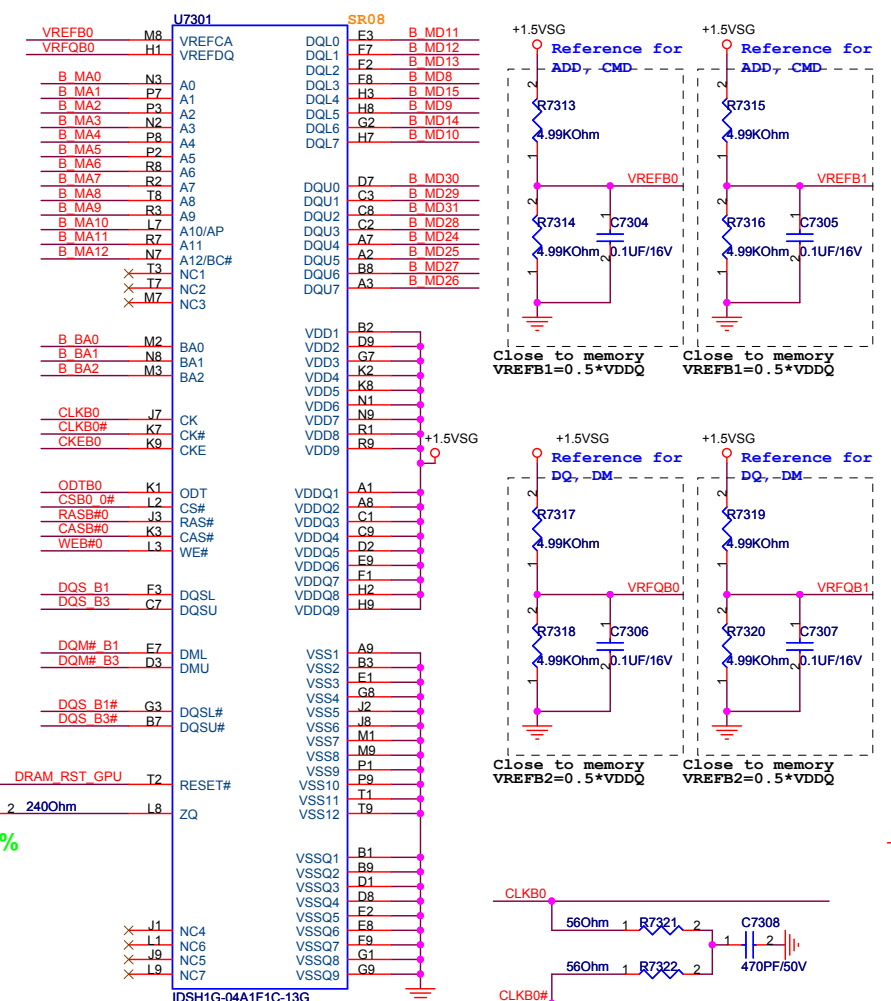
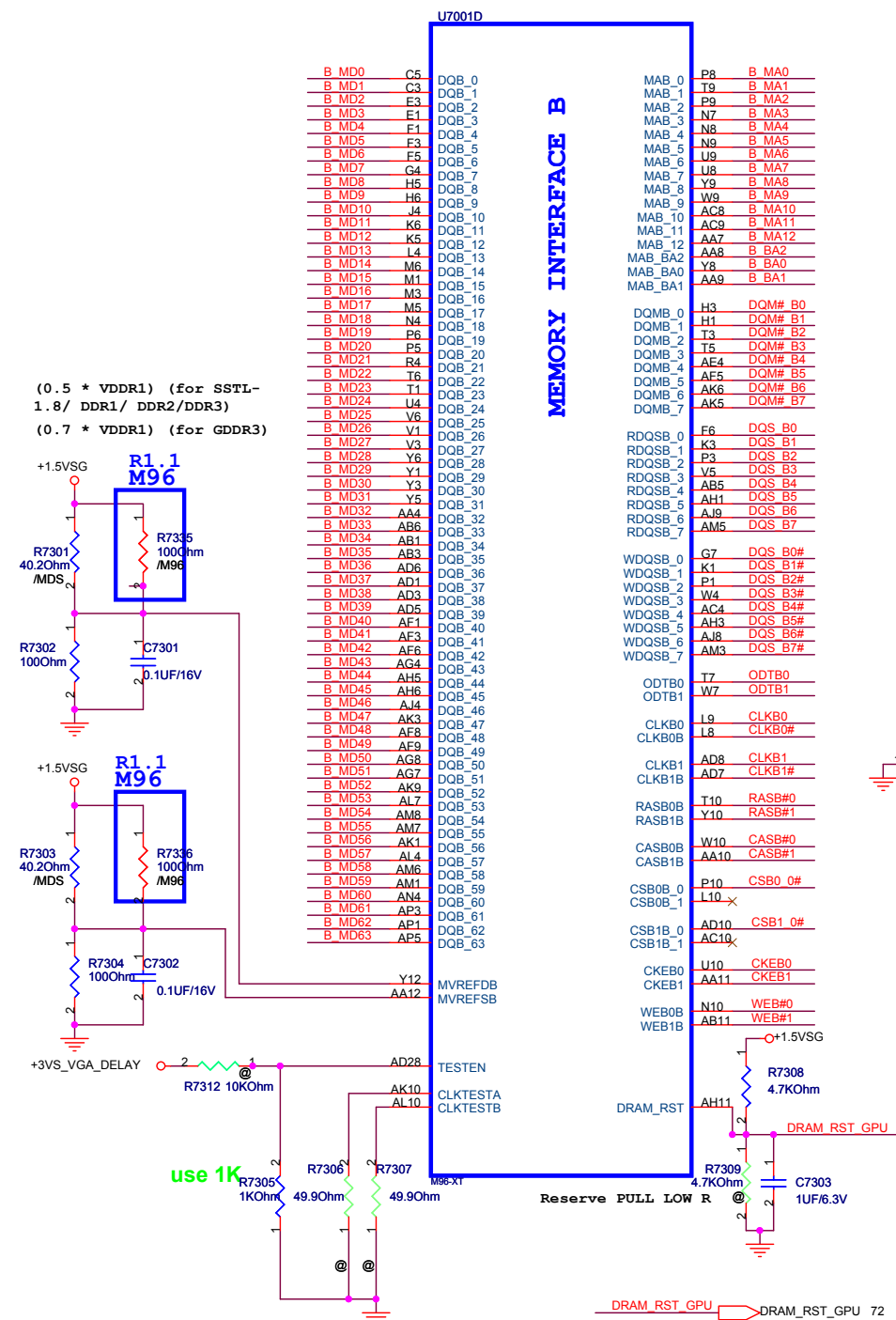
Close to HDMI connector



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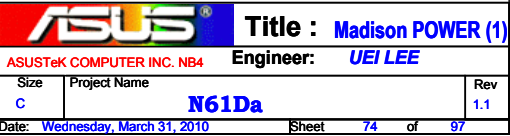






ORCAD SYMBOL:03G151638110  
03G151638020 64M\*16-1.2 FBGA-96 SAMSUNG/K4W1G1646E-HC12  
03G151638421 64M\*16-1.2 FBGA-96 HYNIX/H5TQ1G63BFR-12C



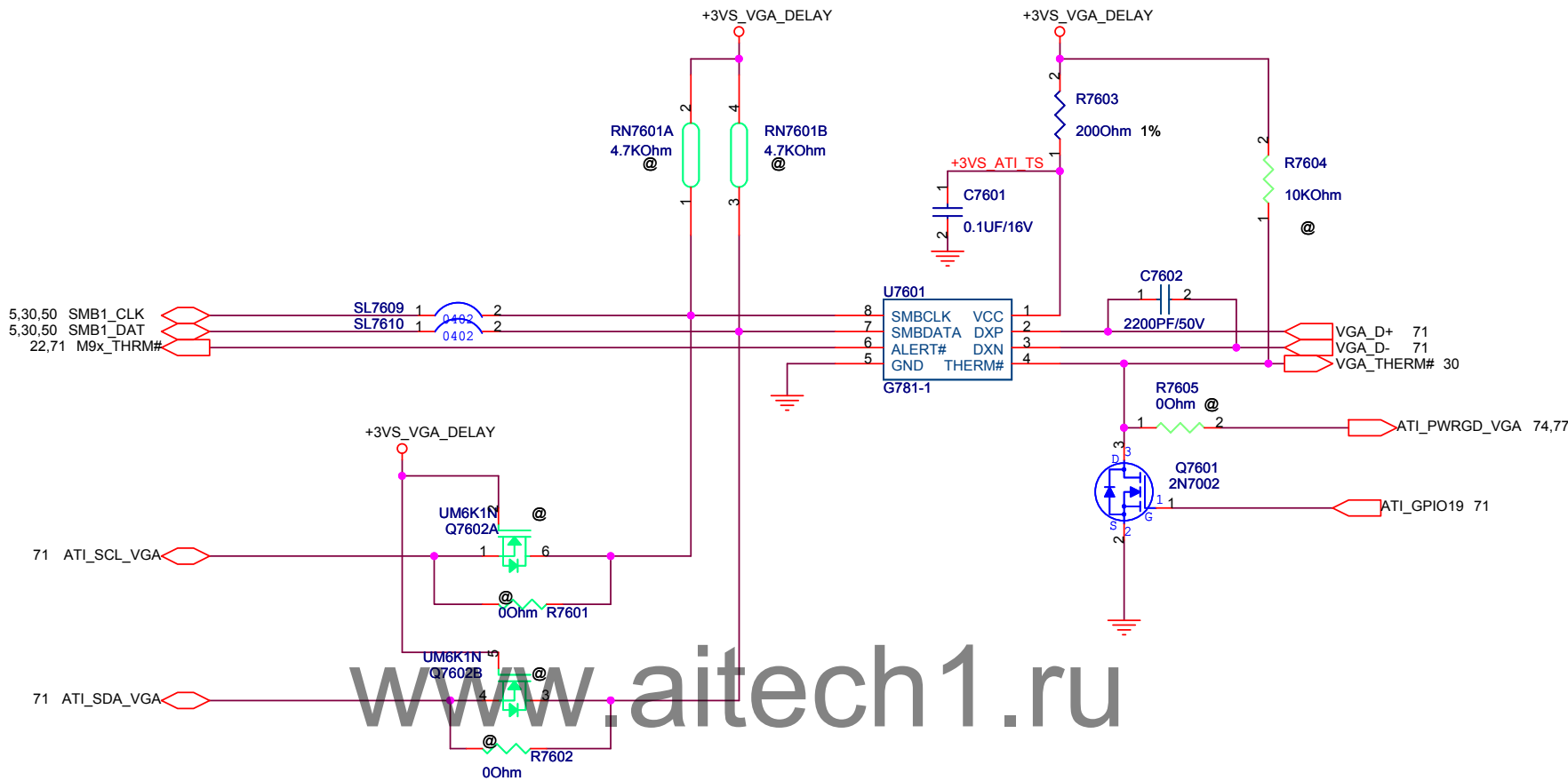




THERMAL SENSOR

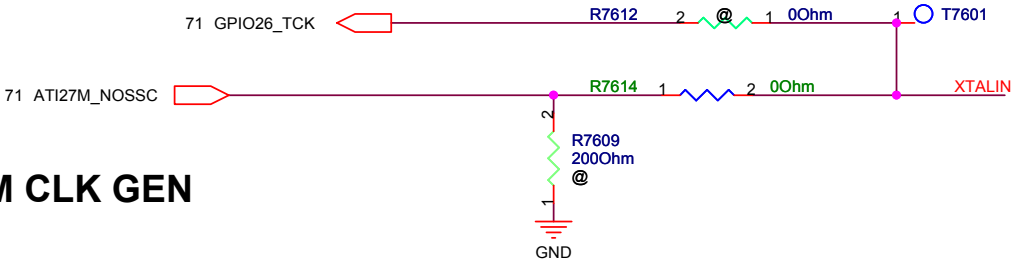
Reserved:  
SMBus, Alert (ICH7): turn on FAN  
Overtemp (ICH7): Windows  
Shutdown

	SMBUS SLAVE ADDRESS
G781	4C ( 1 0 0 1 1 0 0 )
G781-1	4D ( 1 0 0 1 1 0 1 )

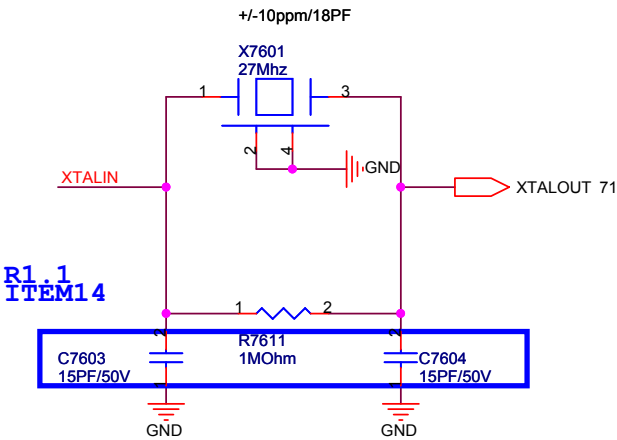


Memory Clock SS  
(Reserved)

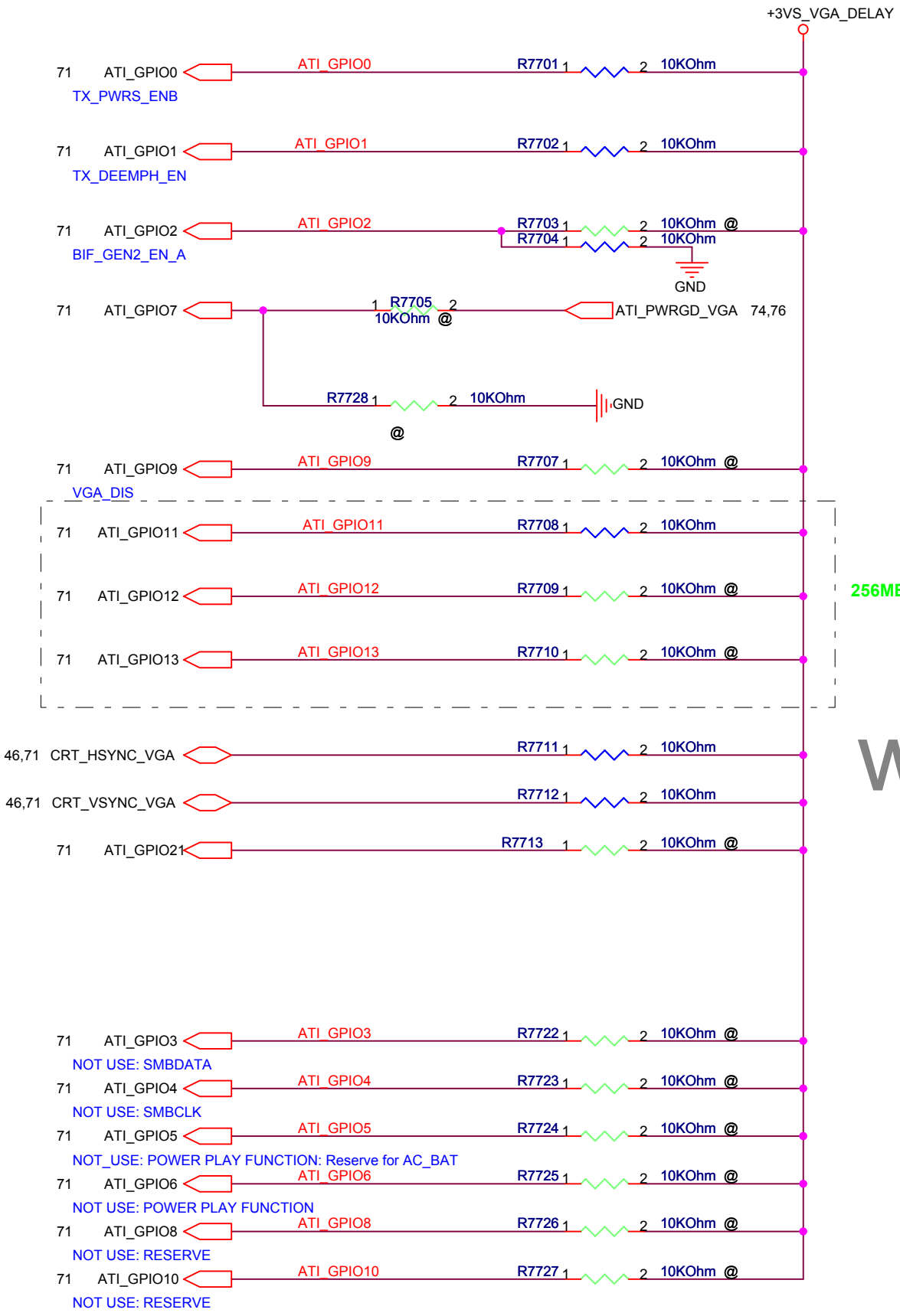
FROM CLK GEN



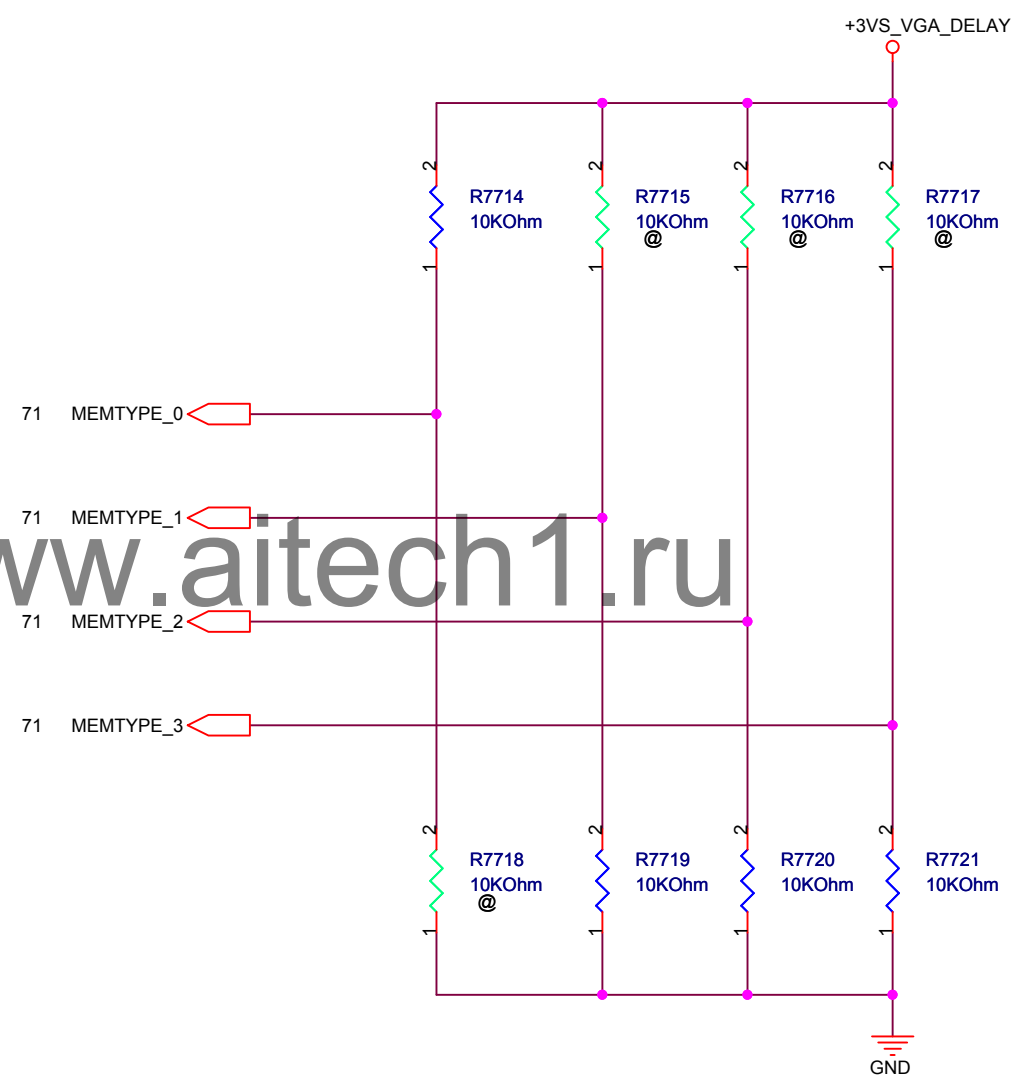
R7612,R7614,R7610,R7613  
CLOSE X7601



OPTION STRAPS



Memory ID Board Straps				
Vendor	DVPDATA(3,2,1,0)	ID	DDR2 Memory Type	Channel Size
Samsung	0000	0	64M*16 (1G)	2-AB channel
Hynix	0001	1	64M*16 (1G)	2-AB channel



0011-03G151638110  
QIMONDA/IDSH1G-04A1F1C-13G  
DDR3 1333 64M\*16-1.5 TFBGA-96  
Mount: VR353, VR22, VR40, VR31  
Unmount: VR352, VR21, VR41, VR27

1111-03G151638210  
ELPIDA/EDJ1116BASE-DJ-E  
DDR3 1333 64M\*16-1.5 FBGA-96  
Mount: VR31, VR40, VR21, VR352  
Unmount: VR27, VR41, VR22, VR353

0101-03G151638013  
Samsung/K4W1G1646D-EC15  
DDR3 1333 64M\*16-1.5 FBGA-100  
Mount: VR353, VR21, VR41, VR31  
Unmount: VR352, VR22, VR40, VR27

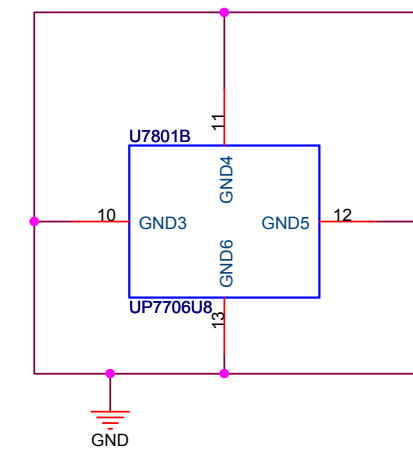
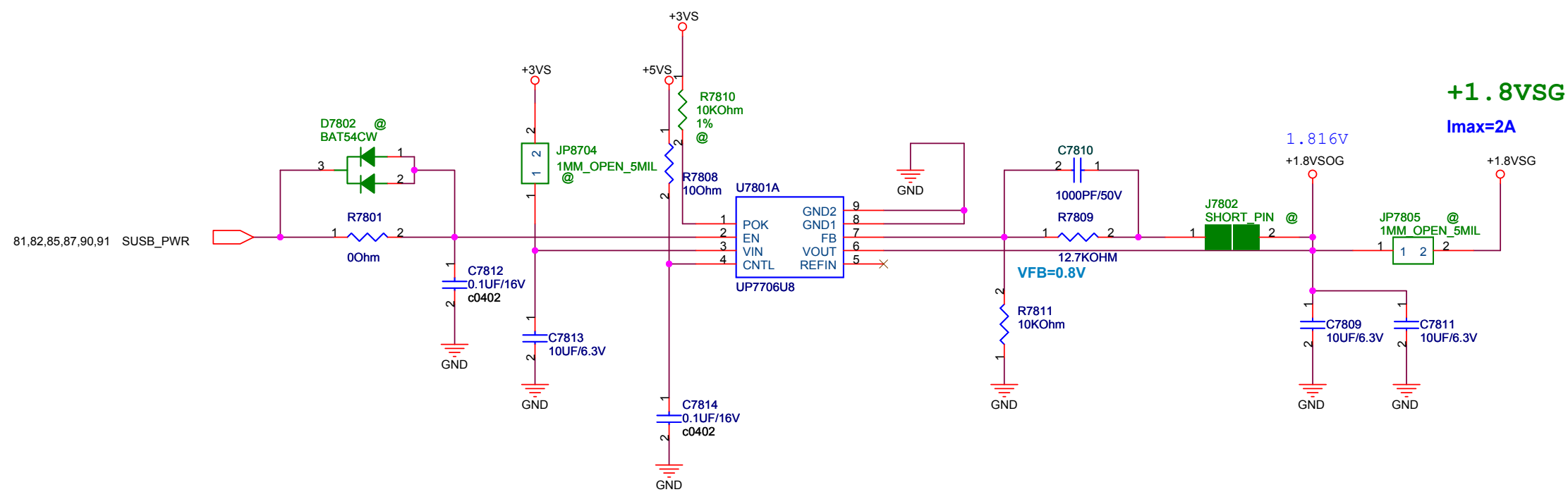
1011-  
DDR3 Hynix (TBD)

MADISON +1.05VSG=1.0V R7820=39.2K  
M96 =1.1V R7820=31.6K

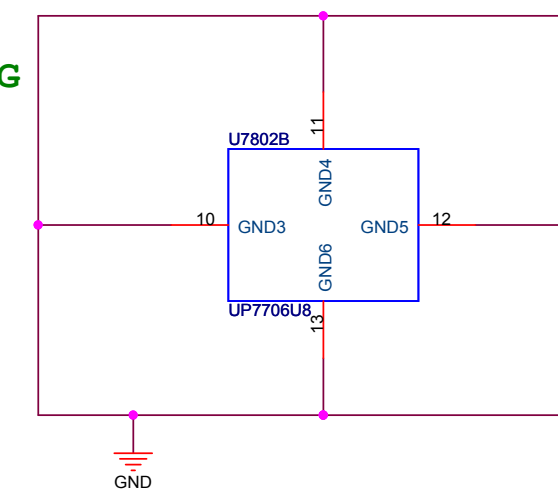
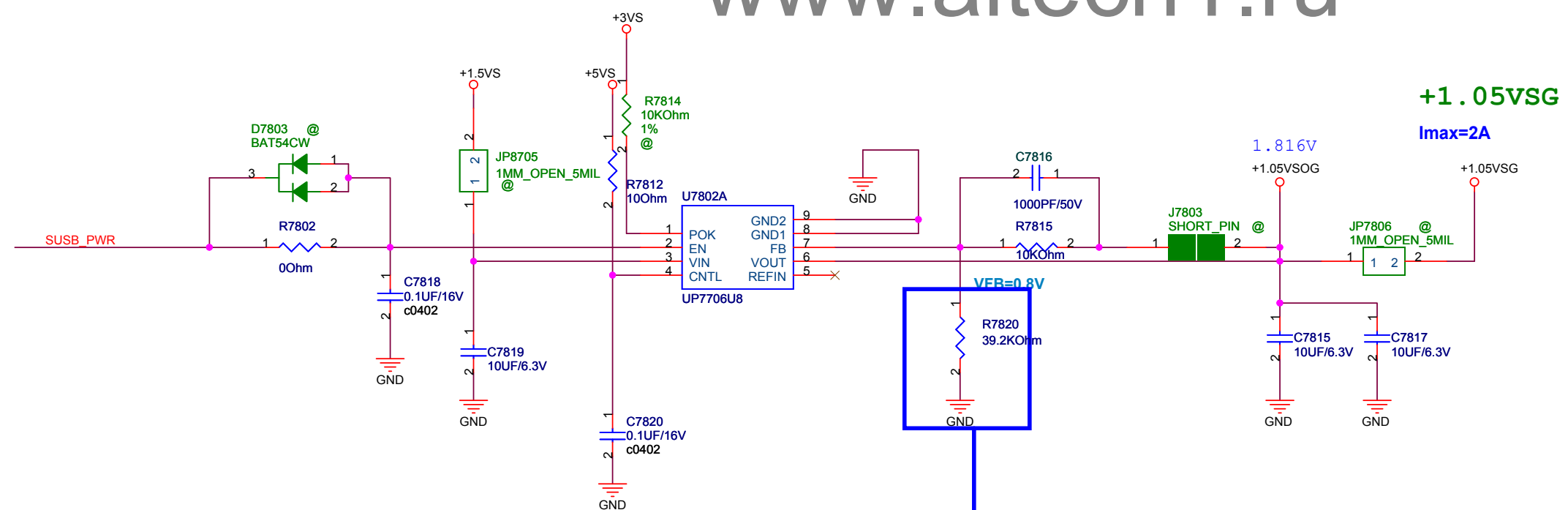
Title : **Madison STRAPS**

ASUSTeK COMPUTER INC. NB4 Engineer: **Uei Lee**

Size <b>B</b>	Project Name <b>N61Da</b>	Rev <b>1.1</b>
Date: <b>Wednesday, March 31, 2010</b>		Sheet <b>77</b> of <b>97</b>



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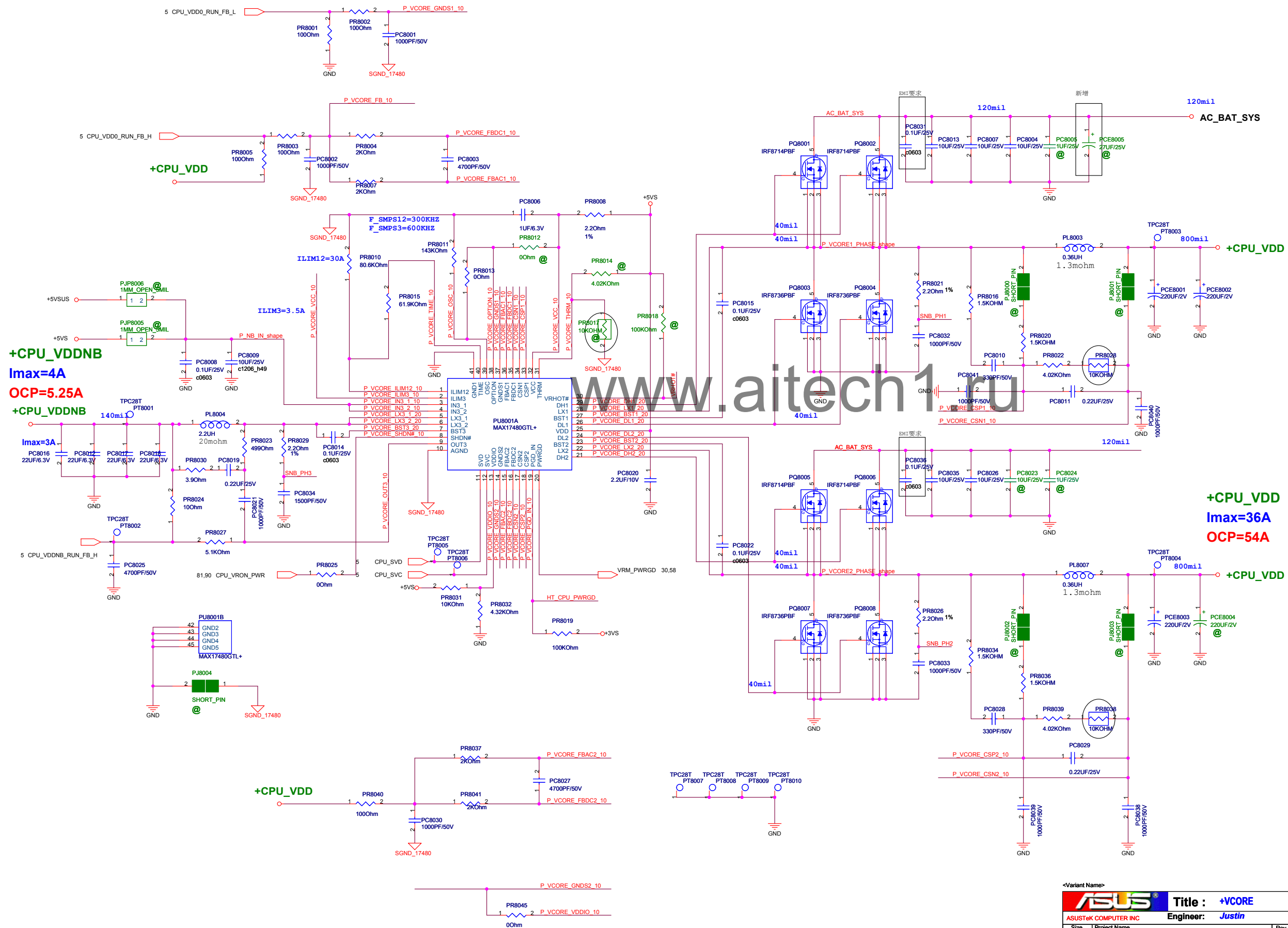
R1.1 ITEM10  
MADISON +1.05VSG=1.0V R7820=39.2K  
M96 =1.1V R7820=26.6K

R1.2

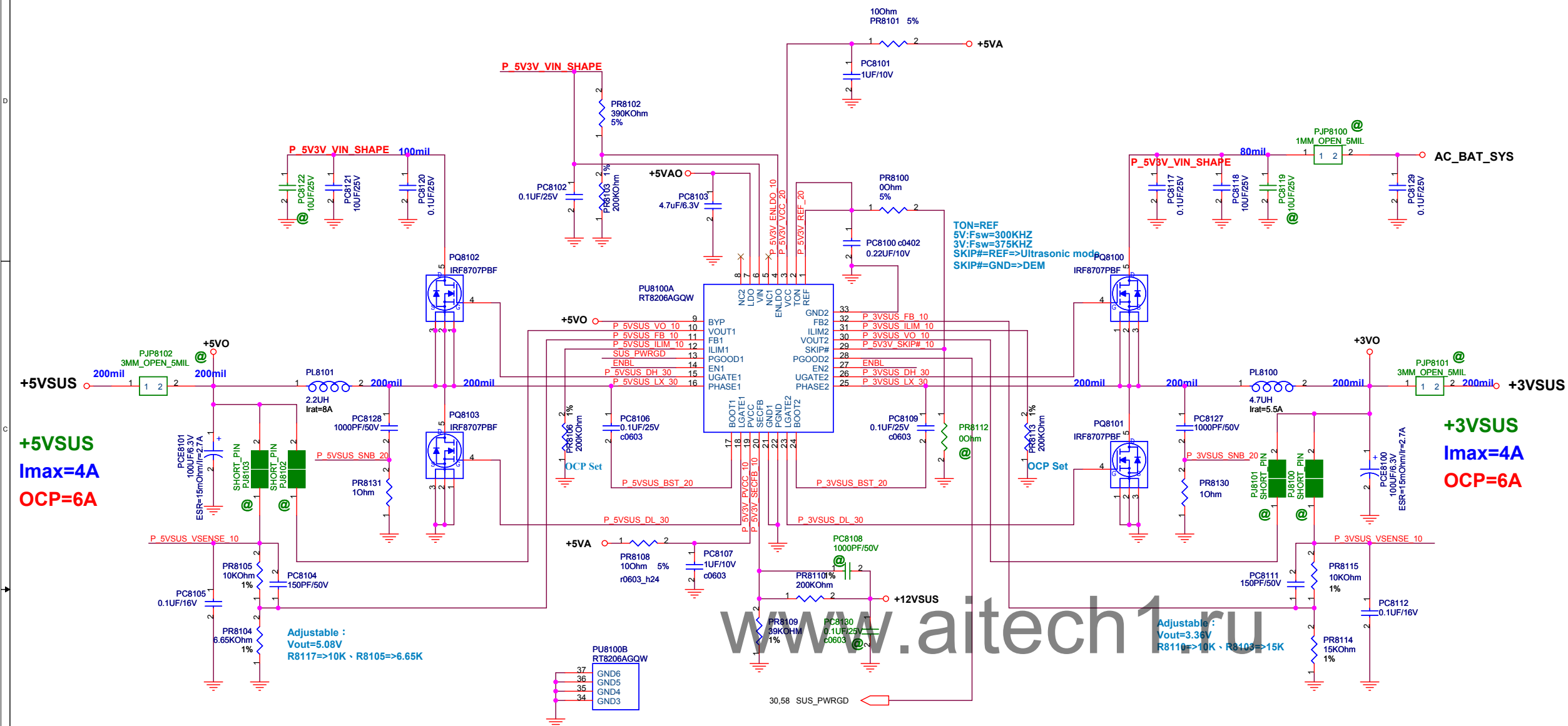


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		Title : <b>VGA_****</b>	
ASUSTeK COMPUTER INC. NB4		Engineer: <b>Uei Lee</b>	
Size <b>B</b>	Project Name <b>N61Da</b>		Rev <b>1.1</b>
Date: <b>Tuesday, March 30, 2010</b>		Sheet <b>79</b> of <b>97</b>	1

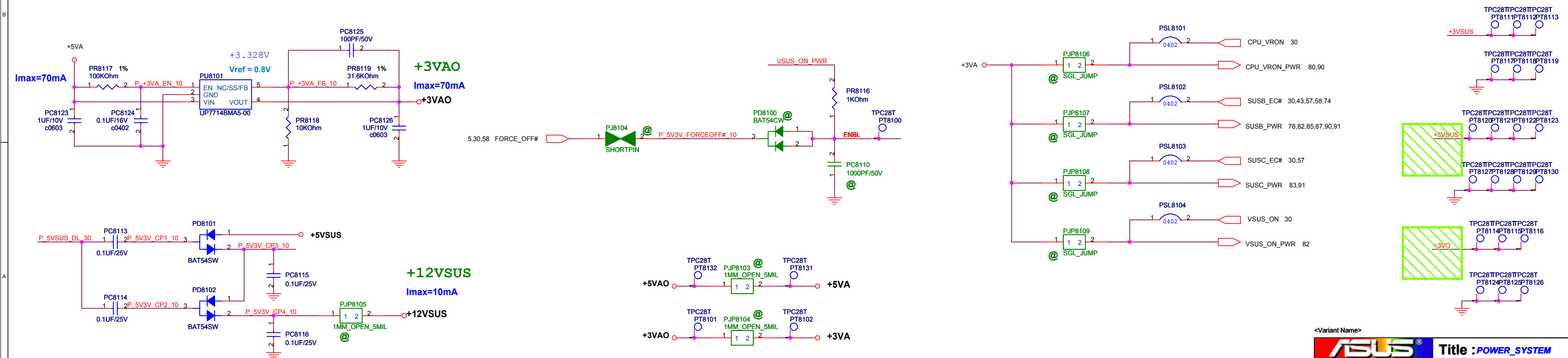


# +5VSUS / +3VSUS POWER SUPPLY

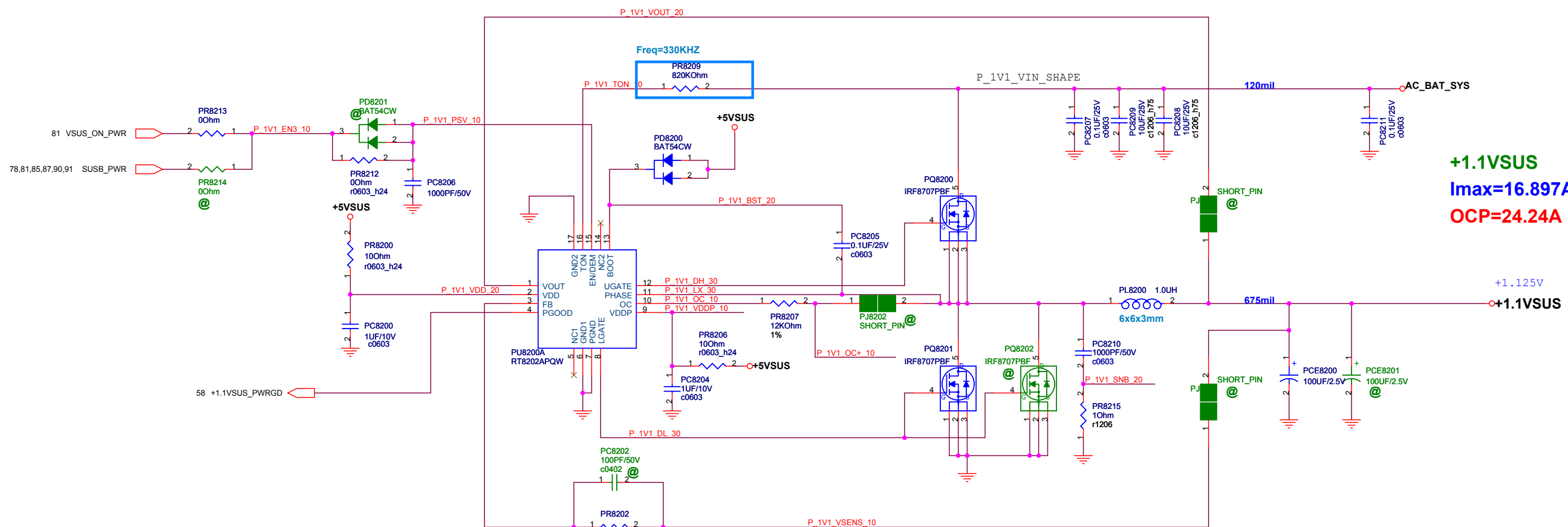


Power stage	
<b>+5VSUS:</b>	<b>+3VSUS:</b>
1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.96A$	1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.96A$
2. Ripple Current: $I_{rip} = 2.61A$	2. Ripple Current: $I_{rip} = 1.55A$
3. Ripple Voltage: $ESR/1 = 15mohm$ $V = 39.15mV$	3. Ripple Voltage: $ESR/1 = 15mohm$ $V = 23.25mV$
4. Inductor Spec: $I_{sat} = 6.2A$ $I_{dc} = 4.6A$ $DCR = 36mohm$	4. Inductor Spec: $I_{sat} = 6.2A$ $I_{dc} = 4.6A$ $DCR = 36mohm$
5. MOSFET Spec: H-side MOSFET: FDMC8884	
$R_{ds(ON)} = 30mohm$ $I_{cont} = 9A$ $I_{peak} = 15A$	$(V_{gs} = 4.5V)$ $(T = 25^\circ C)$ $(Pause = 10\mu s)$
L-side MOSFET: FDMC8884	
$R_{ds(ON)} = 30mohm$ $I_{cont} = 9A$ $I_{peak} = 15A$	$(V_{gs} = 4.5V)$ $(T = 25^\circ C)$ $(Pause = 10\mu s)$

Controller	
<b>+5VSUS:</b>	<b>+3VSUS:</b>
1. Voltage & Current: <b>+5VSUS: 5V / 4A</b>	1. Voltage & Current: <b>+3VSUS: 3.3V / 4A</b>
2. Frequency: <b>F=300KHZ</b>	2. Frequency: <b>F=375KHZ</b>
3. OCP: Set PR8106=357 Kohm $I_{ocp} = 5uA \cdot R_{ocp} / 10 \cdot R_{ds(on)}$ $I_{ocp} = 6A$	3. OCP: Set PR8113=357 Kohm $I_{ocp} = 5uA \cdot R_{ocp} / 10 \cdot R_{ds(on)}$ $I_{ocp} = 6A$
4. Soft start time: The Soft Start duration is 2ms	4. Inrush Current: $C_{total} = 100\mu F$ $I_{inrush} = C \cdot V_{out} / SS\_time$ $I_{inrush} = 0.165A$
5. Inrush Current: $C_{total} = 100\mu F$ $I_{inrush} = C \cdot V_{out} / SS\_time$ $I_{inrush} = 0.165A$	



# +1.1VSUS POWER SUPPLY

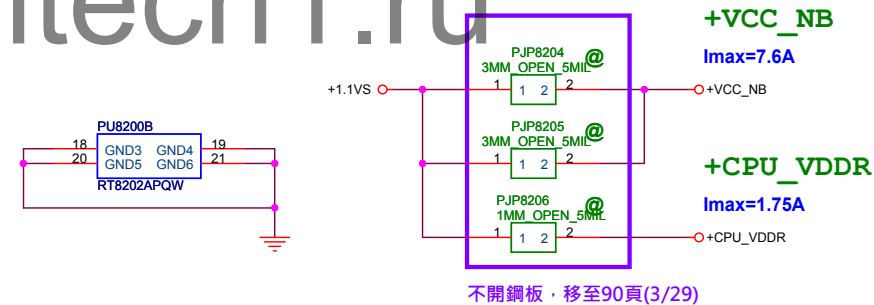


PT8202	TPC28T
+1.1VSUS	1
PT8203	TPC28T
+1.1VSUS	1
PT8204	TPC28T
GND	1
PT8205	TPC28T
GND	1

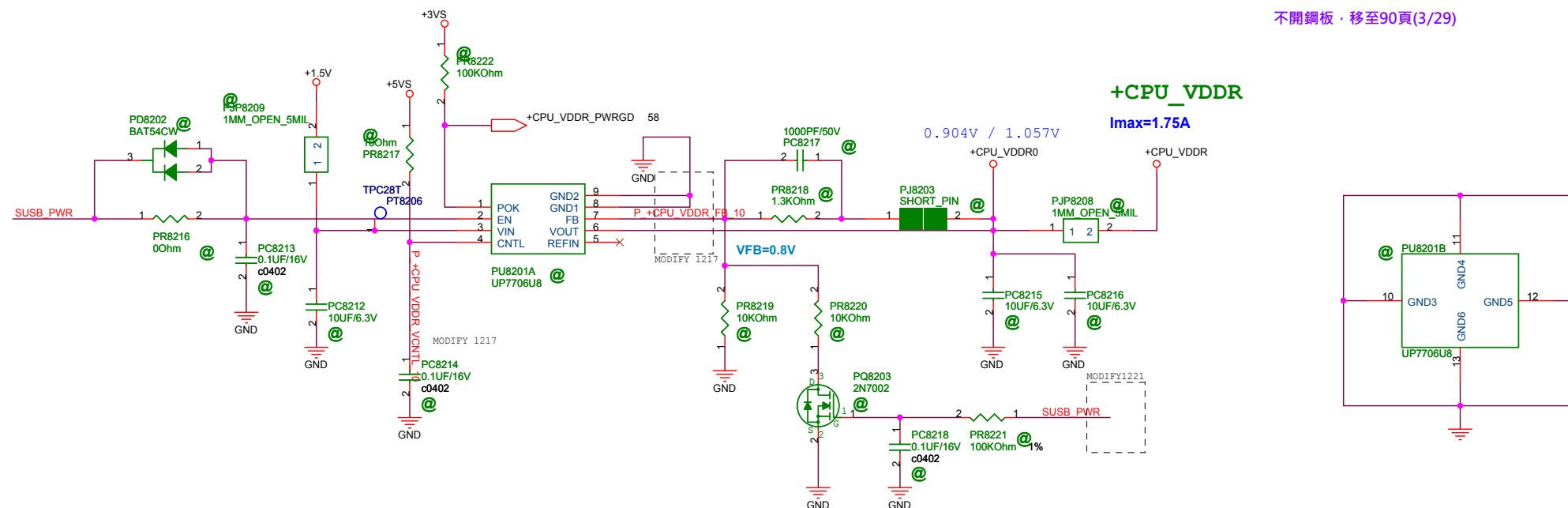
**+1.1VSUS**  
**Imax=16.897A**  
**OCP=24.24A**

Controller
+VTT_CPU:
1. Voltage & Current:
+VTT_CPU: 1.05V / 15A
2. Frequency:
F=330KHZ
3. OCP:
Set PR8207=4.99 Kohm
locp=Rocp*20uA/Rds(on)
locp=26A
4. Soft start time:
The SS duration is 1.35ms
5. Inrush Current:
C total = 440 uF
I inrush=C*Vout/SS_time
I inrush= 0.342 A

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不開鋼板·移至90頁(3/29)

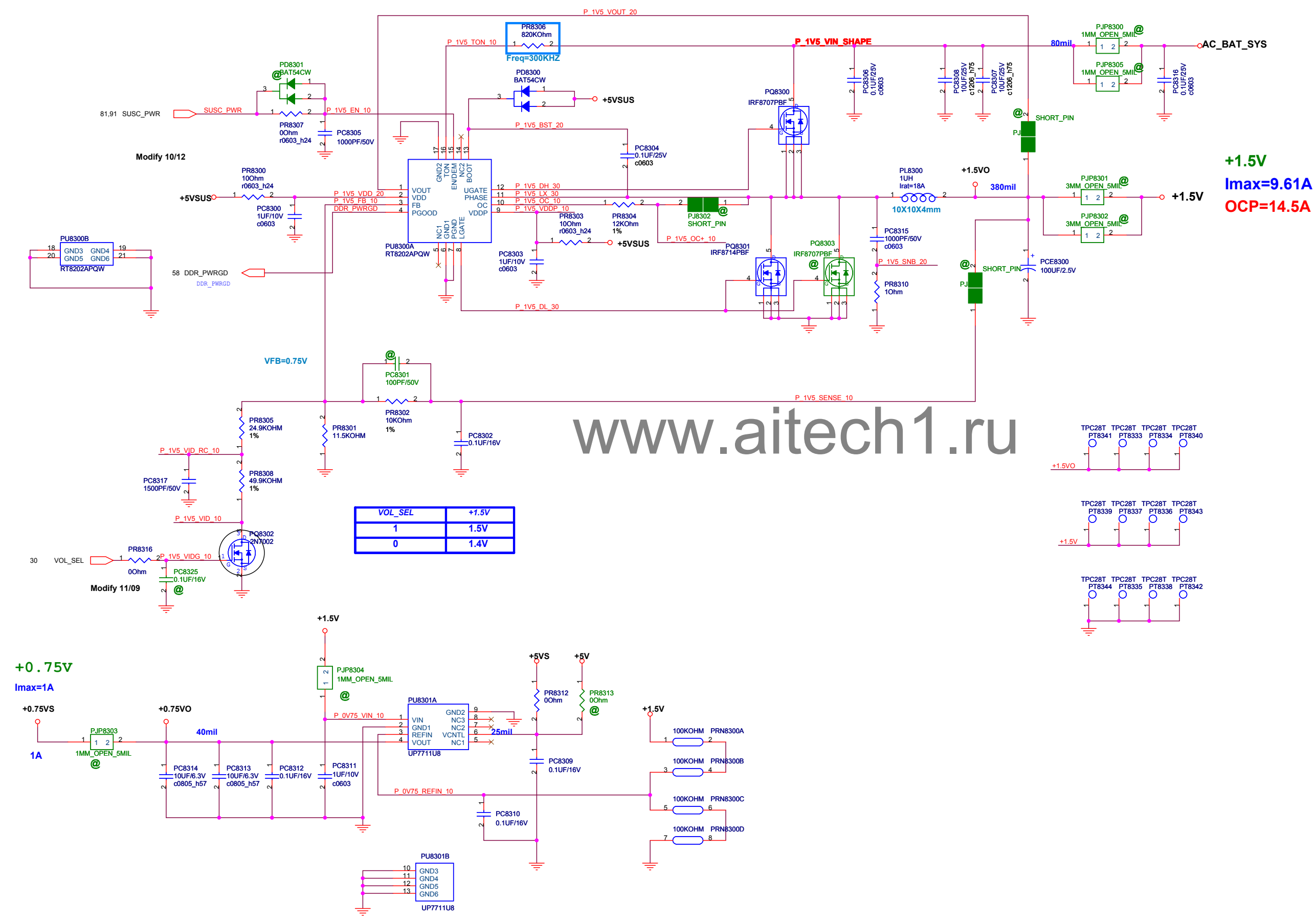


Power stage
+VTT_CPU:
1. I/P Current:
Iin=Vo*Io/(0.75*Vin)=2.33A
2. Ripple Current:
Irip=5.36A
3. Ripple Voltage:
ESR/2=7.5mohm
Vripple=40.26mV
4. Inductor Spec:
Isat=40A
Idc=25A
DCR=1.6mohm
5. MOSFET Spec:
H-side MOSFET: RJK0355DPA
Rds(ON)=16.5mohm (Vgs=4.5 V)
I cont = 30A (T=25 °C)
I peak =120 A (Pause =10 us)
L-side MOSFET: RJK0353DPA
Rds(ON)=7.6mohm (Vgs=4.5 V)
I cont = 35A (T=25 °C)
I peak =140 A (Pause =10 us)

<Variant Name>

ASUS	Title :POWER_I/O_+VCCP
ASUSTek COMPUTER INC. NB	Engineer: Justin
Size	Project Name
Custom	N61DA
Date: Wednesday, March 31, 2010	Sheet 82 of 95

+1.5V & +0.75VS POWER SUPPLY



Power stage

DDR III:

1. I/P Current:  
 $I_{in}=V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.22A$

2. Ripple Current:  
 $I_{rip} = 4.62A$

3. Ripple Voltage:  
 $ESR/1 = 15mohm$   
 $V = 69.3mV$

4. Inductor Spec:  
 $I_{sat} = 12.7A$   
 $I_{dc} = 9.5A$   
 $DCR = 8.5mohm$

5. MOSFET Spec:

H-side MOSFET: RJK0355DPA

$R_{ds(ON)} = 16.5mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 30A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 120A$  (Pause = 10 us)

L-side MOSFET: RJK0355DPA

$R_{ds(ON)} = 16.5mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 30A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 120A$  (Pause = 10 us)

Controller

DDR III:

1. Voltage & Current:  
 $+1.5V: 1.5V / 10A$

2. Frequency:  
 $F = 300KHZ$

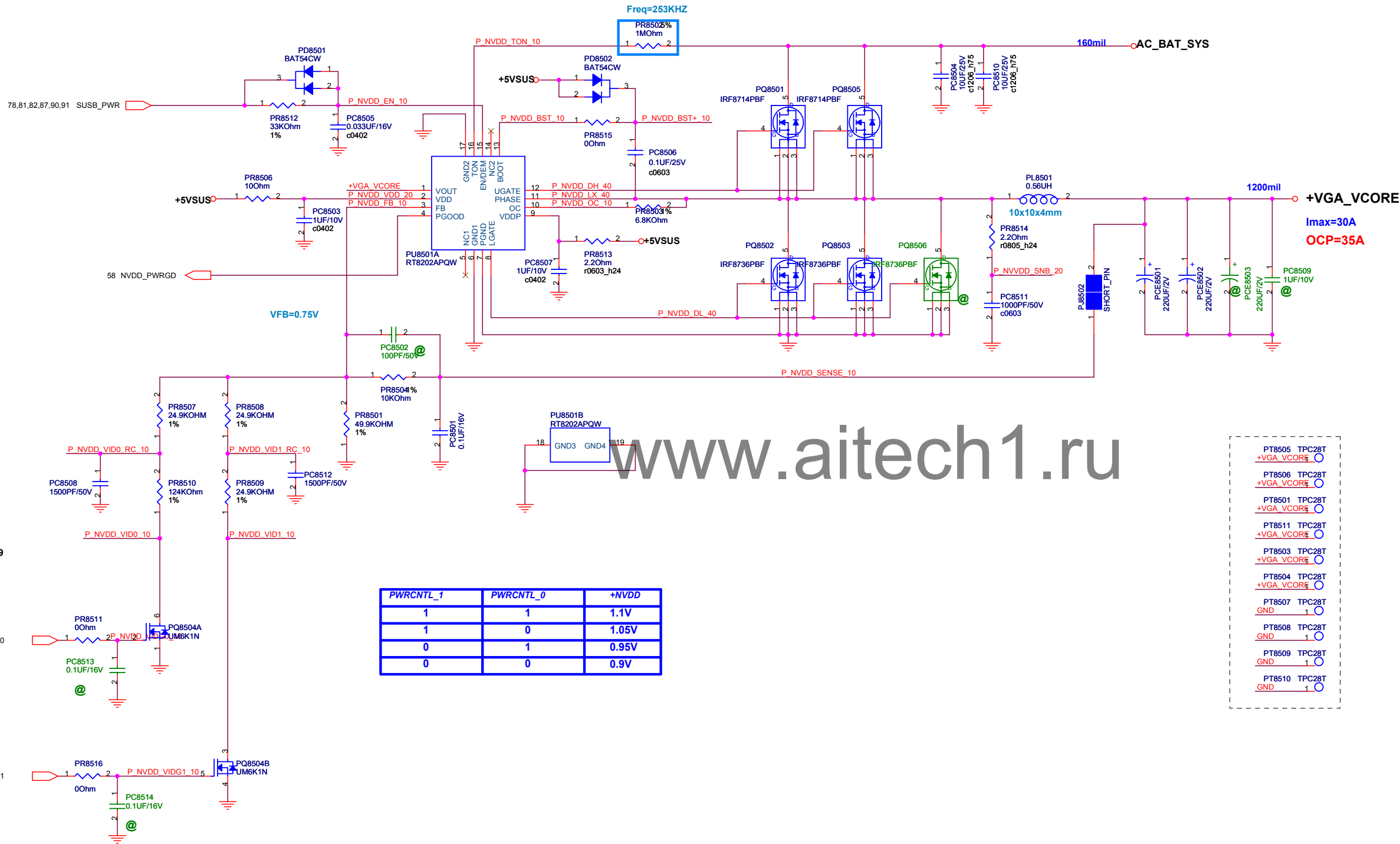
3. OCP:  
Set  $R8302 = 12Kohm$   
 $I_{ocp} = R_{ocp} \cdot 20uA / R_{ds(on)}$   
 $I_{ocp} = 14.3A$

4. Soft start time:  
The Soft Start duration is 1.35ms

5. Inrush Current:  
 $C_{total} = 220uF$   
 $I_{inrush} = C \cdot V_{out} / SS\_time$   
 $I_{inrush} = 0.244A$

1. Voltage & Current:  
 $+0.75V: 0.75V / 1A$

GPU NVDD POWER SUPPLY



**Power stage**

**NVDD:**

- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.11A$
- Ripple Current:**  
 $I_{rip} = 7.31A$
- Ripple Voltage:**  
 $ESR/2 = 3mohm$   
 $V = 21.9mV$
- Inductor Spec:**  
 $I_{sat} = 30.5A$   
 $I_{dc} = 29.5A$   
 $DCR = 1.5mohm$
- MOSFET Spec:**  
**H-side MOSFET: RJK0355DPA**  
 $R_{ds(ON)} = 16.5mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 30A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 120A$  (Pause = 10 us)  
**L-side MOSFET: RJK0353DPA**  
 $R_{ds(ON)} = 7.6mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 35A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 140A$  (Pause = 10 us)

**Controller**

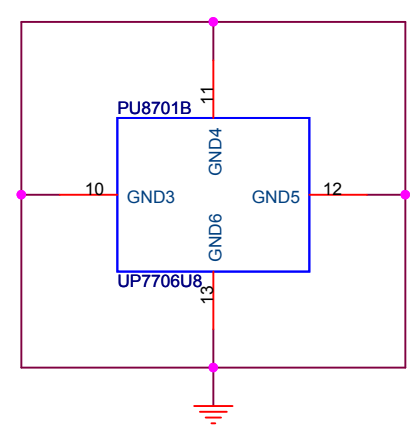
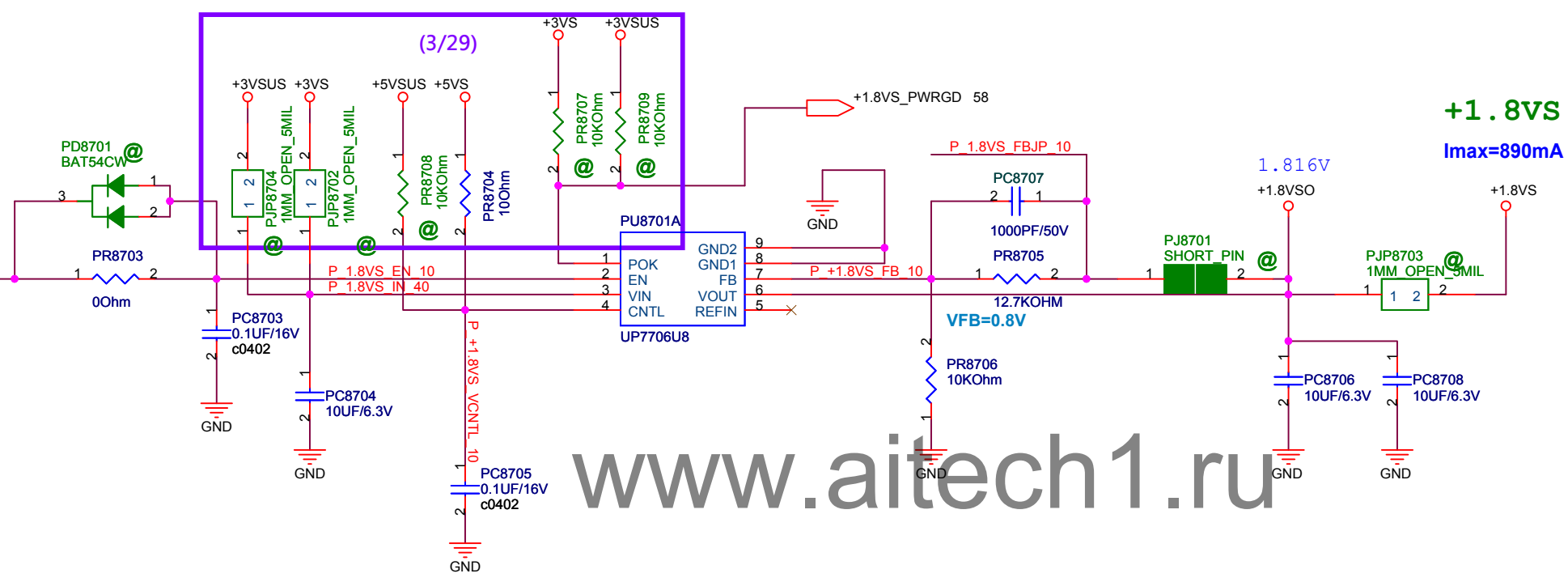
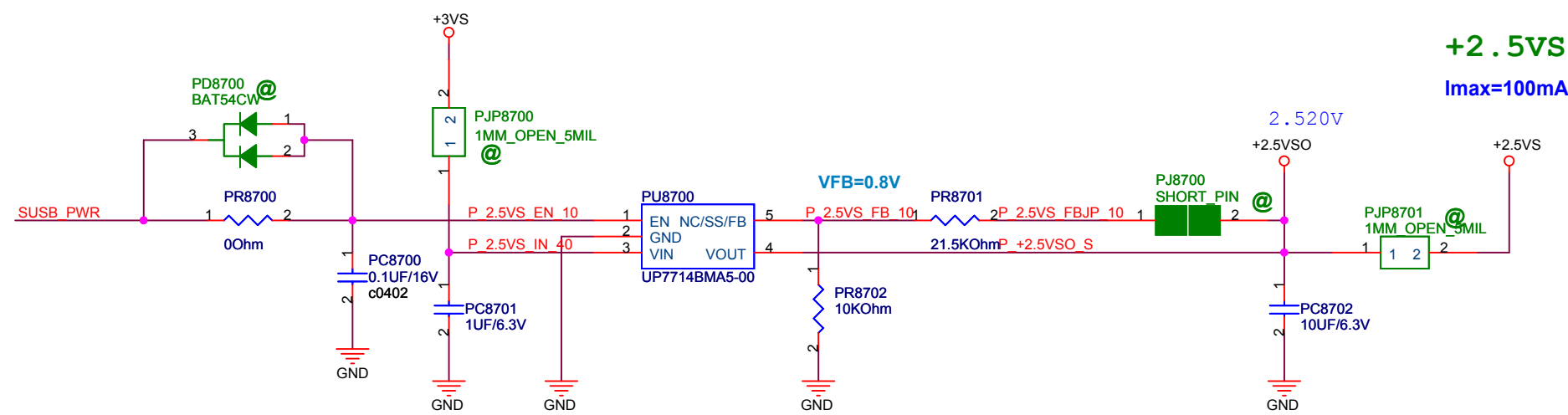
**NVDD:**

- Voltage & Current:**  
**+NVDD: 1.1V / 15A**
- Frequency:**  
**F = 253KHZ**
- OCP:**  
Set R8504 = 6.8 Kohm  
 $I_{ocp} = R_{ocp} \cdot 20uA / R_{ds(on)}$   
 $I_{ocp} = 35A$
- Soft start time:**  
The Soft Start duration is 1.35ms
- Inrush Current:**  
 $C_{total} = 660uF$   
 $I_{inrush} = C \cdot V_{out} / SS\_time$   
 $I_{inrush} = 0.537A$

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PWRCNTL_1	PWRCNTL_0	+NVDD
1	1	1.1V
1	0	1.05V
0	1	0.95V
0	0	0.9V

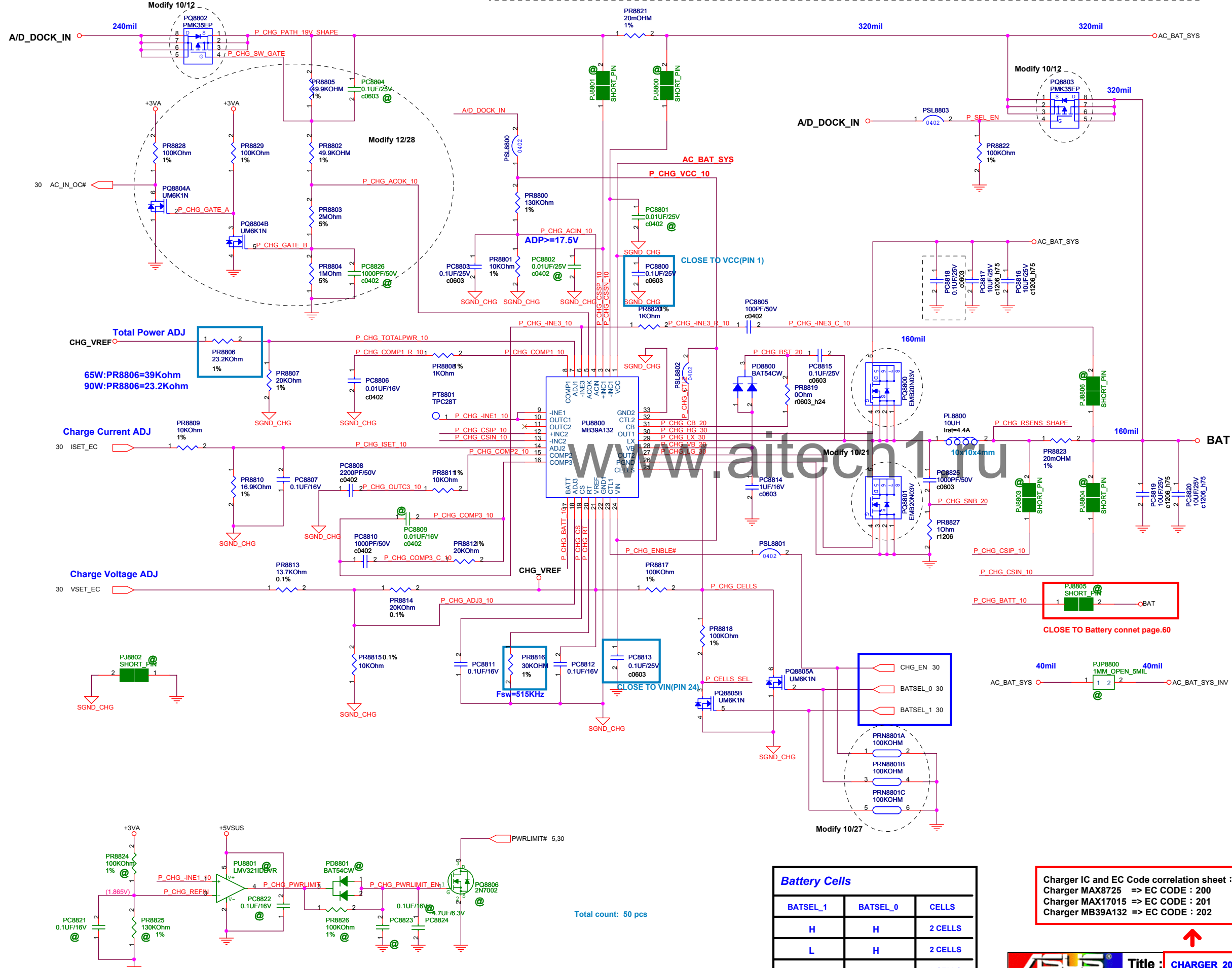
- PT8505 TPC28T +VGA\_VCORE
- PT8506 TPC28T +VGA\_VCORE
- PT8501 TPC28T +VGA\_VCORE
- PT8511 TPC28T +VGA\_VCORE
- PT8503 TPC28T +VGA\_VCORE
- PT8504 TPC28T +VGA\_VCORE
- PT8507 TPC28T GND
- PT8508 TPC28T GND
- PT8509 TPC28T GND
- PT8510 TPC28T GND



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PT8802 TPC28T	PT8805 TPC28T	PT8808 TPC28T	PT8811 TPC28T	PT8814 TPC28T	PT8817 TPC28T	PT8820 TPC28T	PT8823 TPC28T	PT8826 TPC28T	PT8828 TPC28T
AC_BAT_SYS 1	AC_BAT_SYS 1	A/D_DOCK_IN 1	A/D_DOCK_IN 1	BAT 1	BAT 1	BATSEL_0 1	AC_IN_OCR 1	PWRLIMIT# 1	GND 1
PT8803 TPC28T	PT8806 TPC28T	PT8809 TPC28T	PT8812 TPC28T	PT8815 TPC28T	PT8818 TPC28T	PT8821 TPC28T	PT8824 TPC28T	PT8827 TPC28T	PT8829 TPC28T
AC_BAT_SYS 1	AC_BAT_SYS 1	A/D_DOCK_IN 1	A/D_DOCK_IN 1	BAT 1	BAT 1	BATSEL_1 1	ISET_EC 1	GND 1	GND 1
PT8804 TPC28T	PT8807 TPC28T	PT8810 TPC28T	PT8813 TPC28T	PT8816 TPC28T	PT8819 TPC28T	PT8822 TPC28T	PT8825 TPC28T	PT8831 TPC28T	PT8830 TPC28T
AC_BAT_SYS 1	AC_BAT_SYS 1	A/D_DOCK_IN 1	A/D_DOCK_IN 1	BAT 1	BAT 1	CHG_EN 1	VSET_EC 1	GND 1	GND 1



**Battery Cells**


BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

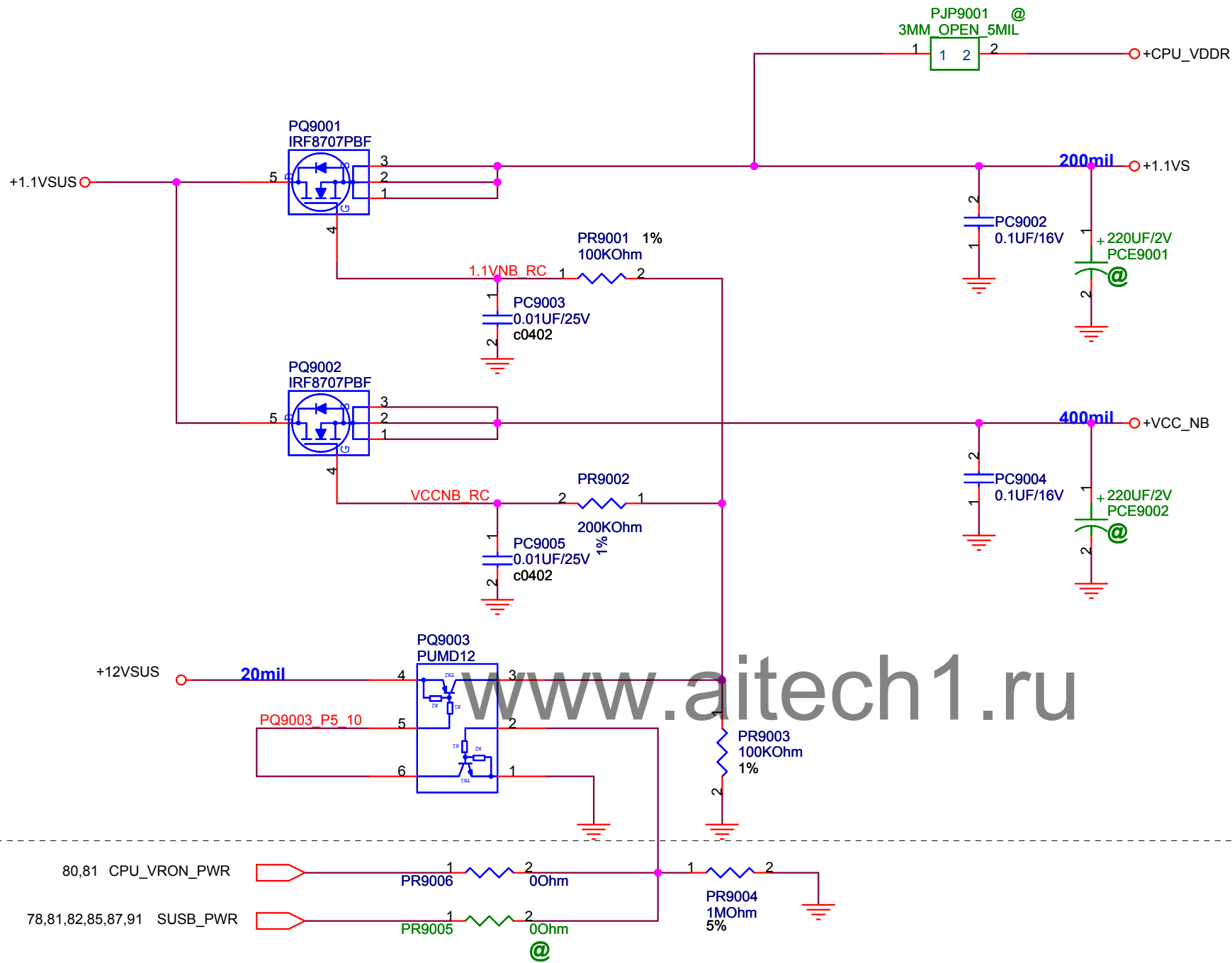
Charger IC and EC Code correlation sheet :  
 Charger MAX8725 => EC CODE : 200  
 Charger MAX17015 => EC CODE : 201  
 Charger MB39A132 => EC CODE : 202



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<Variant Name>

		Title :	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
Custom	Oemga		R1.0
Date: Tuesday, March 30, 2010		Sheet	89 of 95

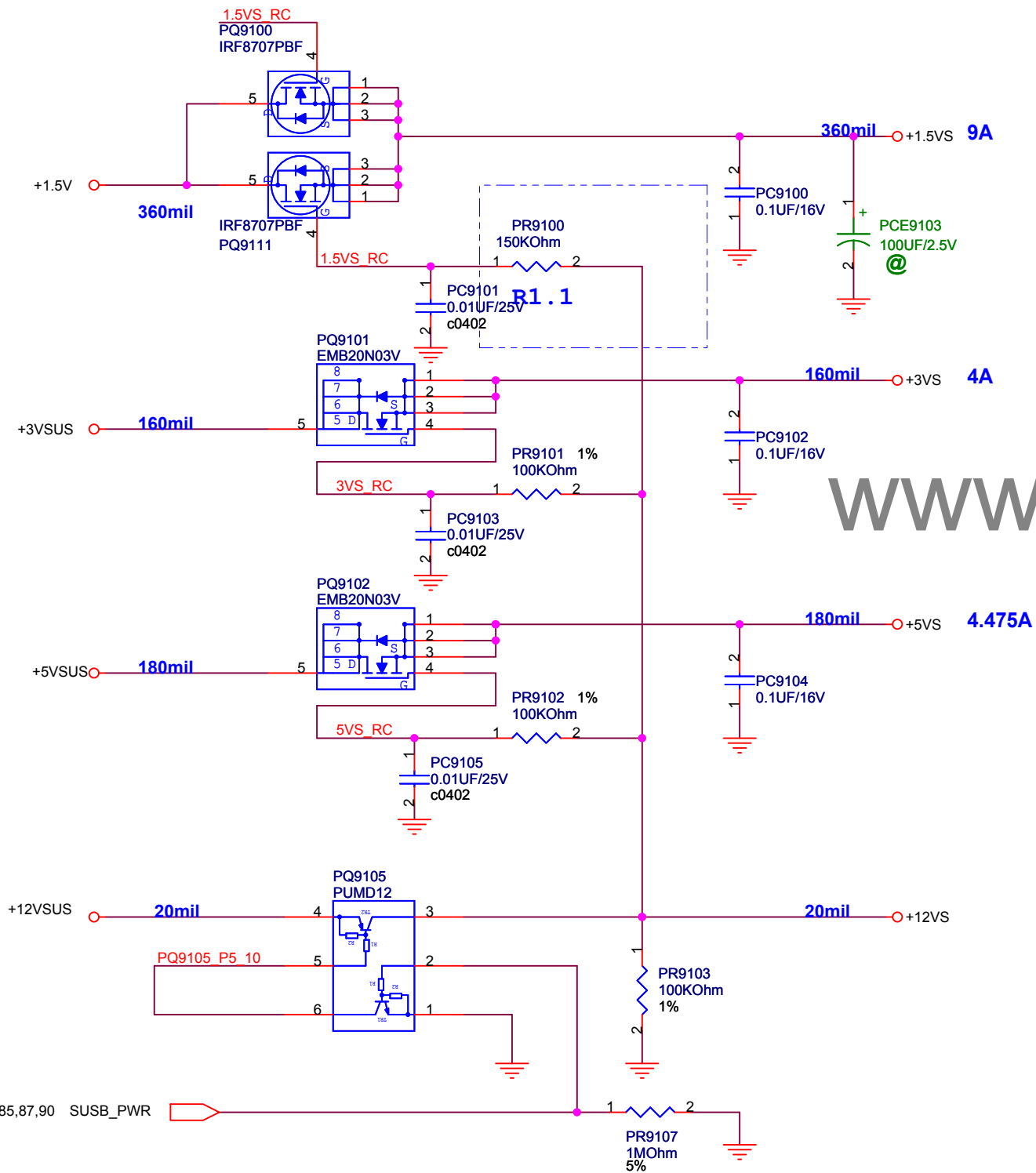


<Variant Name>

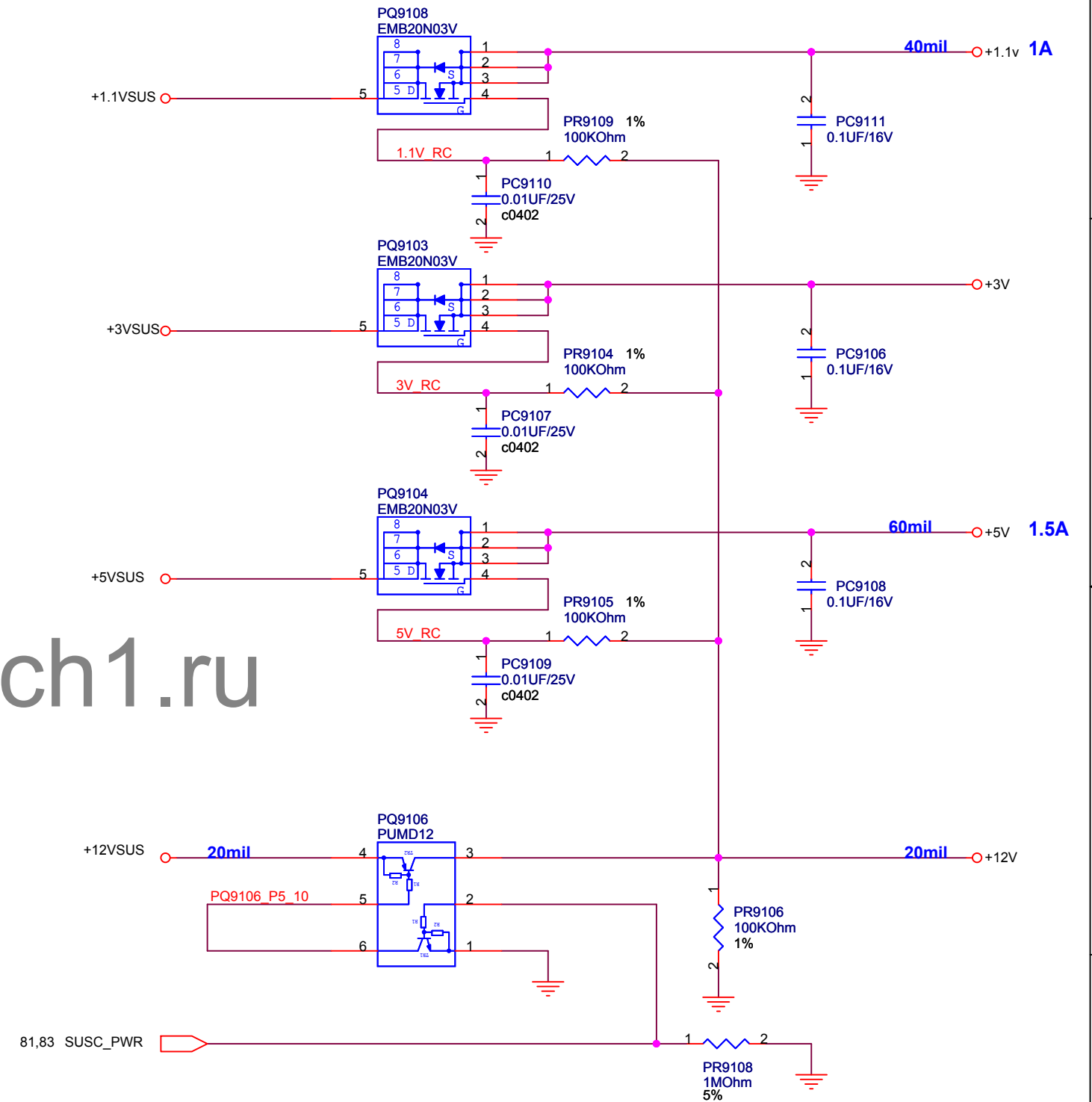
ASUS®		Title : <b>PW_LOAD SW 1.1VSUS</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <b>Eason</b>	
Size Custom	Project Name <b>K72DR</b>		Rev 1.0
Date: <b>Wednesday, March 31, 2010</b>		Sheet <b>90</b> of <b>95</b>	

# SUSB\_PWR POWER

MODIFY0329



# SUSC\_PWR POWER




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<Variant Name>

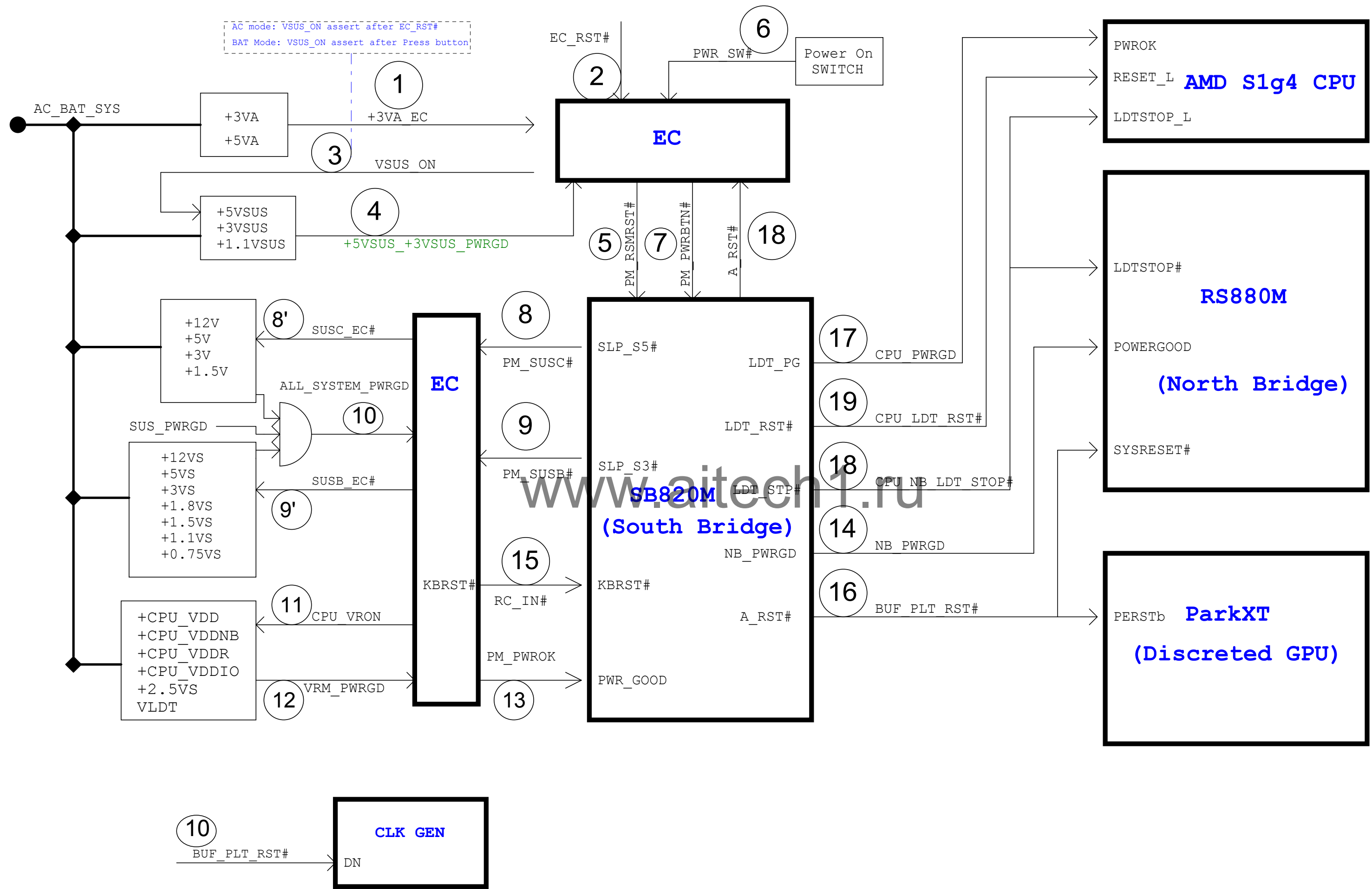
<b>ASUS</b>		<b>Title : POWER_LOAD SWITCH</b>	
ASUSTeK COMPUTER INC. NB		Engineer: Justin	
Size B	Project Name N61DA		Rev R1.0
Date: Wednesday, March 31, 2010		Sheet 91	of 95

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R10

		Title :	
ASUSTek Computer INC.		Engineer:	
Size Custom	Project Name N61DA		Rev 1.1
Date: Tuesday, March 30, 2010		Sheet 92 of 95	






R1.1 CHANGE LIST  
ITEM NO:  
M96. 加入M96相容線路.  
1. Change R2305 to L2324  
2. Mount R5321 and R5322  
3. Add HDMI common choke for EMI. Page 48.  
4. Change Q5803 to IREF8736. Page 58  
5. Add U1201 to improve CPU\_LDTSTOP# signal quality.  
6. Mount R2029  
7. DFM要求刪除COLAY的HALL SENSOR.  
8. Change +1.5VSG source from +1.5V to +1.5VS.  
9. Change BAT1\_IN\_OC# pull high from 10K ohm to 100k ohm.  
10. Chage R7820 to 39.2K for Madison; 31.6K for M96  
11. Change CL of X2001.  
12. Change CL of X2002.  
13. Change CL of X6801.  
14. Change CL of X7601.  
15. Modify Power on sequence.  
16. Mount C4011 for EMI.  
18. Change CPU\_THRMTRIP# pull high from +3VS to +3VSUS.  
19. Add Q2102.  
20. Change R6803 to 6.2K and add R6815.


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		Title : System History	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size Custom	Project Name N61Da		Rev
Date: Tuesday, March 30, 2010		Sheet 96 of 97	



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		<b>Title :</b> System History	
ASUSTeK COMPUTER INC. NB		<b>Engineer:</b>	
Size A	Project Name N61Da		Rev
Date: Tuesday, March 30, 2010		Sheet	97 of 97